

2PG011

Silicon N-channel enhancement IGBT

For plasma display panel drive

For high speed switching circuits

■ Features

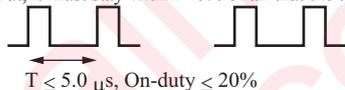
- Low collector-emitter saturation voltage: $V_{CE(sat)} < 2.5 \text{ V}$
- High-speed switching: $t_f = 185 \text{ ns}$ (typ.)

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-emitter voltage (E-B short)	V_{CES}	540	V
Gate-emitter voltage (E-B short)	V_{GES}	-30 to +35	V
Collector current	I_C	40	A
Peak collector current *	I_{CP}	230	A
Power dissipation	P_C	40	W
		$T_a = 25^\circ\text{C}$ 2.0	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *: Assurance of repetitive pulse. (Repetitive period $\leq 5 \mu\text{s}$ on-duty $\leq 20\%$)

But, it must stay within 40% of all that the time impressed pulse repetitively.



■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	条件	最小	標準	最大	Unit	
Collector-emitter voltage (E-B short)	V_{CES}	$I_C = 1 \text{ mA}$, $V_{GE} = 0$	540			V	
Collector-emitter cutoff current (E-B short) *	I_{CES}	$V_{CE} = 432 \text{ V}$, $V_{GE} = 0$			5.0	μA	
Gate-emitter cutoff current (E-B short)	I_{GES}	$V_{GE} = +35 \text{ V}$, -30 V , $V_{CE} = 0$			± 1.0	μA	
Gate-emitter threshold voltage	$V_{GE(th)}$	$V_{CE} = 10 \text{ V}$, $I_C = 1.0 \text{ mA}$	3.0		5.5	V	
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_{GE} = 15 \text{ V}$, $I_C = 40 \text{ A}$		1.95	2.5	V	
Collector-emitter reverse break down voltage	$-V_{CE}$	$I_C = -100 \text{ mA}$, $V_{GE} = 15 \text{ V}$	18	22.5		V	
Short-circuit input capacitance (Common emitter)	C_{ies}	$V_{CE} = 25 \text{ V}$, $V_{GE} = 0$, $f = 1 \text{ MHz}$		1 210		pF	
Short-circuit output capacitance (Common emitter)	C_{oes}				125		pF
Reverse transfer capacitance (Common emitter)	C_{res}				21		pF
Gate charge load	Q_g	$V_{CC} = 250 \text{ V}$, $I_C = 40 \text{ A}$, $V_{GE} = 15 \text{ V}$		51		nC	
Gate-emitter charge	Q_{ge}				9		nC
Gate-collector charge	Q_{gc}				20		nC
Turn-on delay time	$t_{d(on)}$	$V_{CC} = 250 \text{ V}$, $I_C = 40 \text{ A}$, $RL \approx 6.25 \Omega$, $V_{GE} = 15 \text{ V}$		75		ns	
Rise time	t_r				610		ns
Turn-off delay time	$t_{d(off)}$				200		ns
Fall time	t_f				185	300	ns
Thermal resistance (ch-c)	$R_{th(ch-c)}$				3.13	$^\circ\text{C/W}$	
Thermal resistance (ch-a)	$R_{th(ch-a)}$				63	$^\circ\text{C/W}$	

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *: I_{CES} is 100% tested according to the I_{CES} inspection standards. ($< 1.0 \mu\text{A}$ under the conditions of $V_{CE} = 432 \text{ V}$, $V_{GE} = 0$)

■ Package

• Code

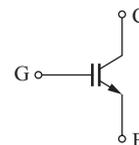
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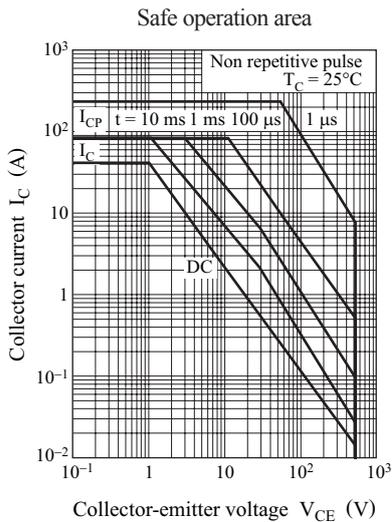
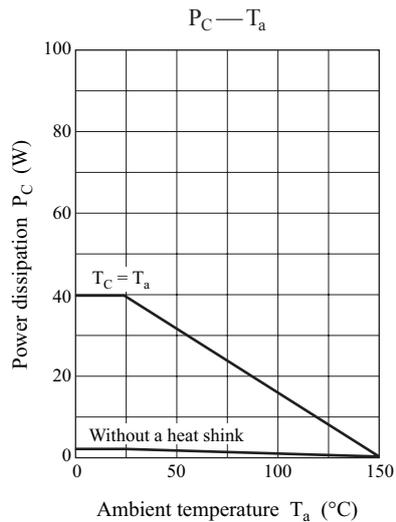
• Pin Name

1. Gate
2. Collector
3. Emitter

■ Marking Symbol: 2PG011

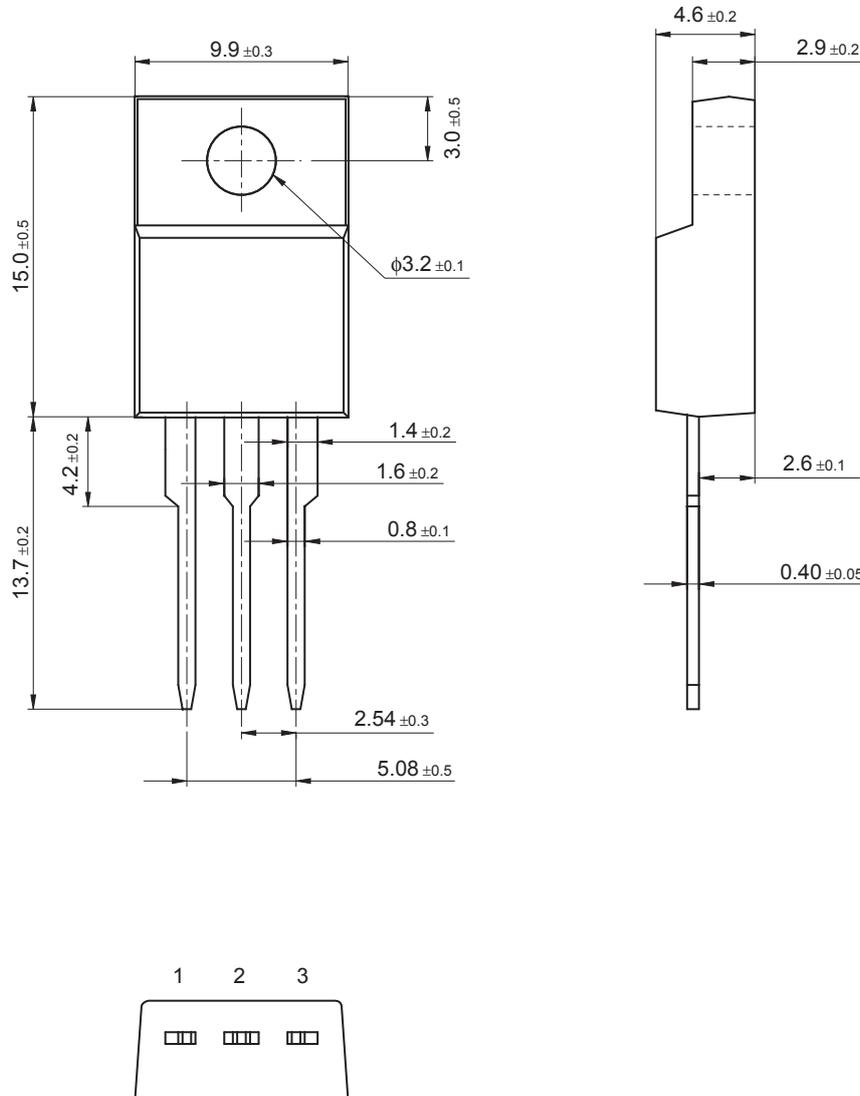
■ Internal Connection





TO-220D-A1

Unit: mm



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