

MOS FIELD EFFECT TRANSISTOR

2SJ598

SWITCHING

P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ598 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low on-state resistance:
 $R_{DS(on)1} = 130 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -6 \text{ A)}$
 $R_{DS(on)2} = 190 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -6 \text{ A)}$
- Low C_{iss} : $C_{iss} = 720 \text{ pF TYP.}$
- Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 12	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 30	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	23	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	-12	A
Single Avalanche Energy ^{Note2}	E_{AS}	14.4	mJ

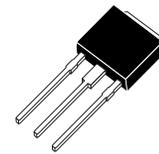
Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = -20 \rightarrow 0 \text{ V}$

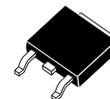
★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ598	TO-251 (MP-3)
2SJ598-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252)

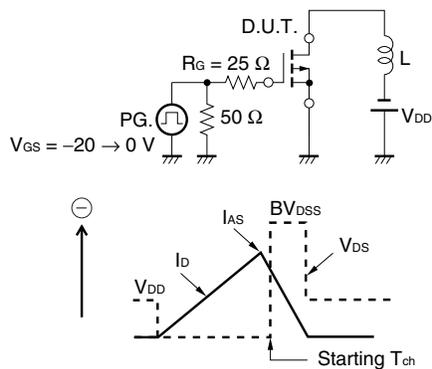


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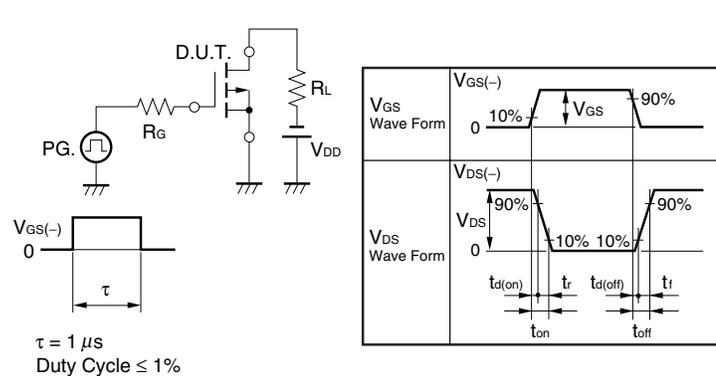
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V$			-10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \mp 16V, V_{DS} = 0V$			∓ 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10V, I_D = -1mA$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10V, I_D = -6A$	5	11		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -10V, I_D = -6A$		102	130	m Ω
	$R_{DS(on)2}$	$V_{GS} = -4.0V, I_D = -6A$		131	190	m Ω
Input Capacitance	C_{iss}	$V_{DS} = -10V$		720		pF
Output Capacitance	C_{oss}	$V_{GS} = 0V$		150		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1MHz$		50		pF
Turn-on Delay Time	$t_{d(on)}$	$I_D = -6A$		7		ns
Rise Time	t_r	$V_{GS} = -10V$		4		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = -30V$		35		ns
Fall Time	t_f	$R_G = 0\Omega$		10		ns
Total Gate Charge	Q_G	$I_D = -12A$		15		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = -48V$		3		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = -10V$		4		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 12A, V_{GS} = 0V$		0.98		V
Reverse Recovery Time	t_{rr}	$I_F = 12A, V_{GS} = 0V$		50		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$		100		nC

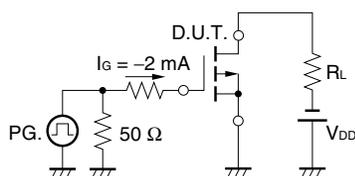
TEST CIRCUIT 1 AVALANCHE CAPABILITY



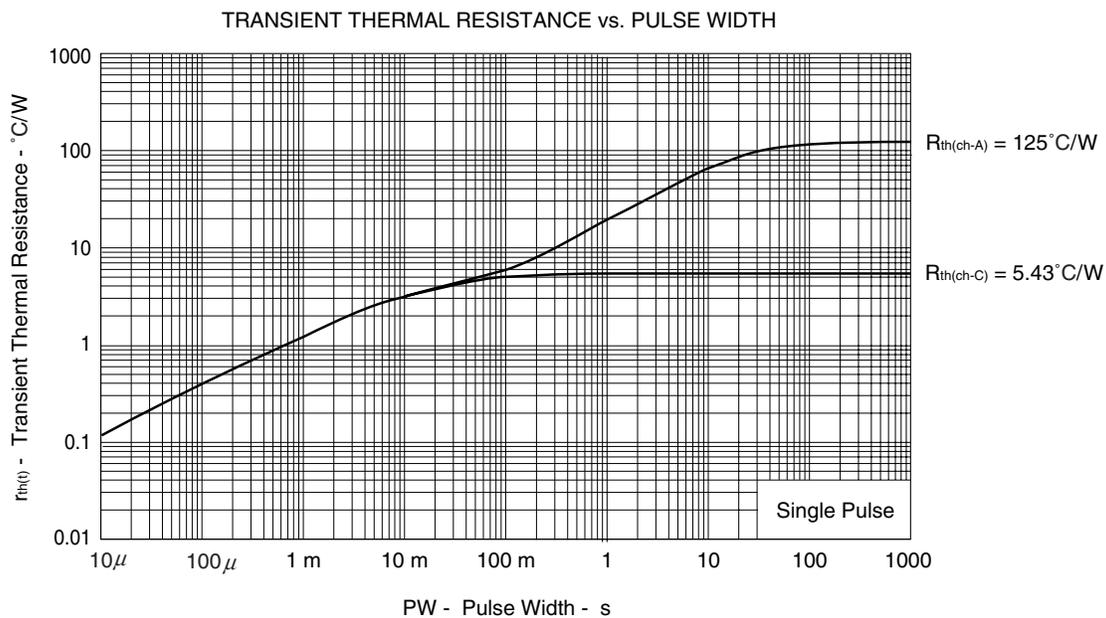
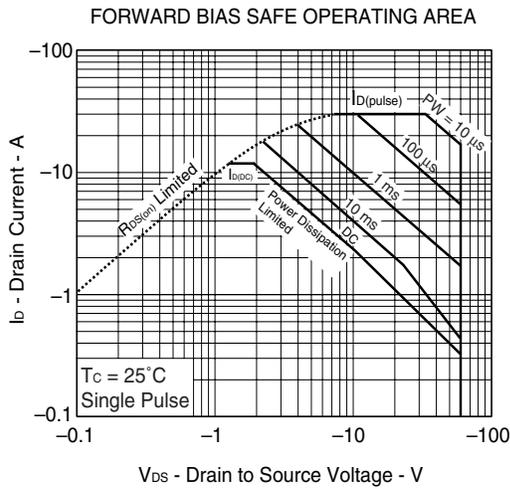
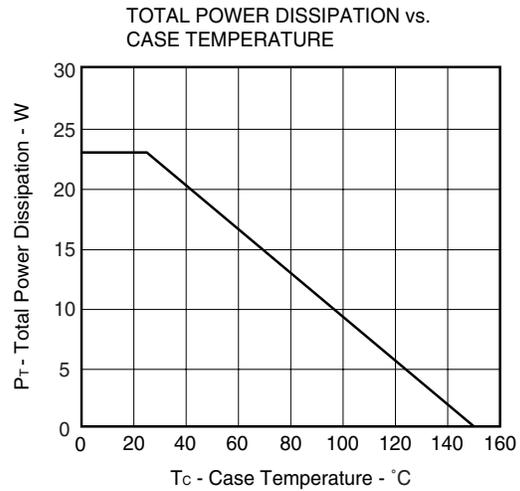
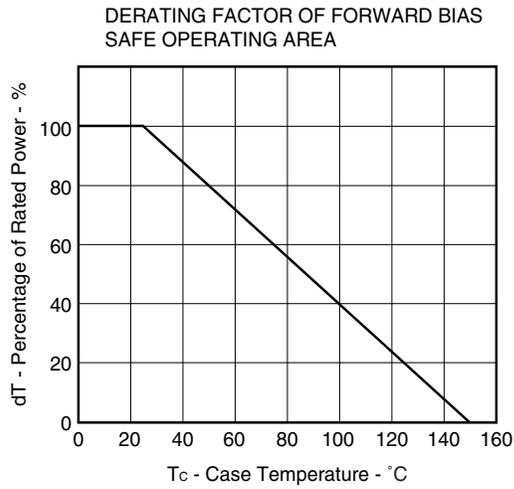
TEST CIRCUIT 2 SWITCHING TIME



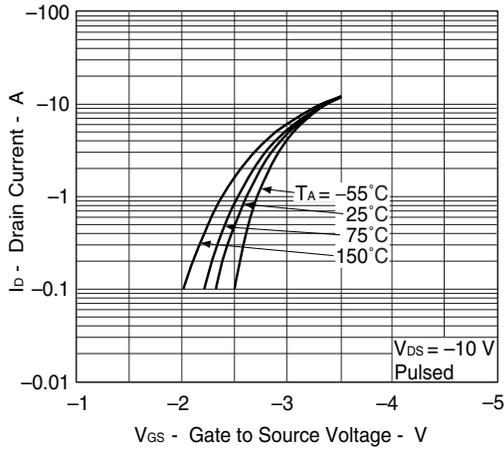
TEST CIRCUIT 3 GATE CHARGE



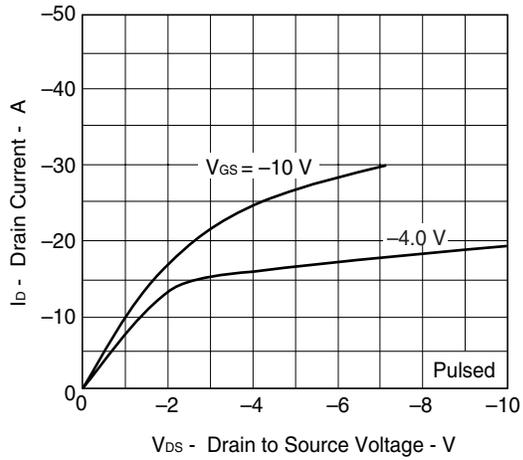
TYPICAL CHARACTERISTICS (T_A = 25°C)



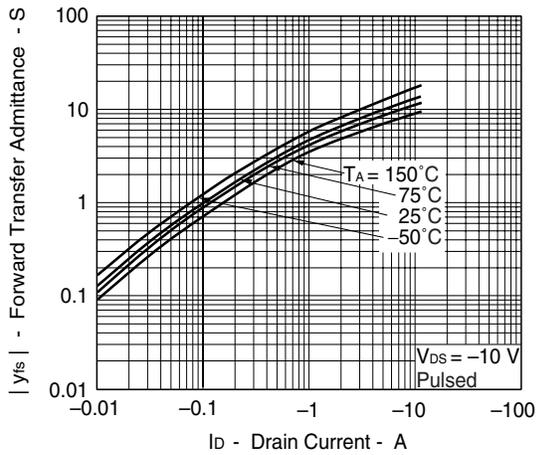
FORWARD TRANSFER CHARACTERISTICS



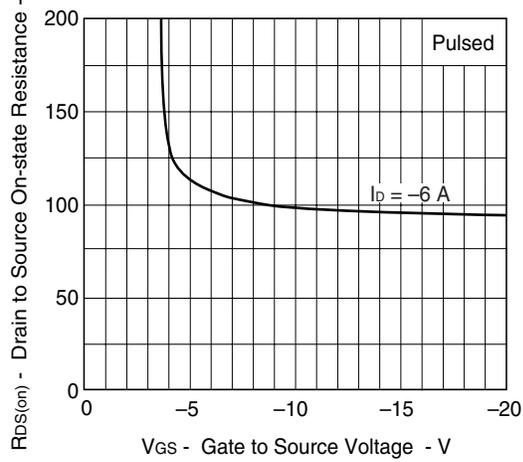
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



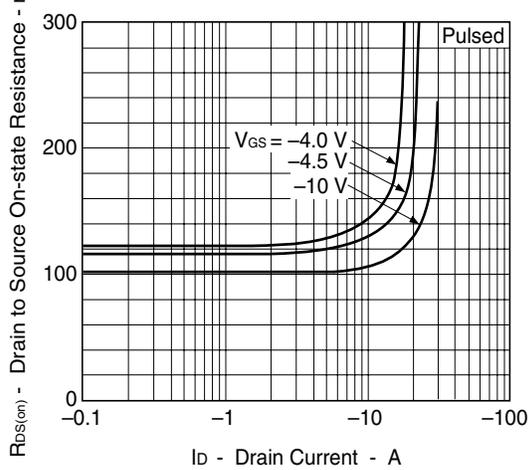
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



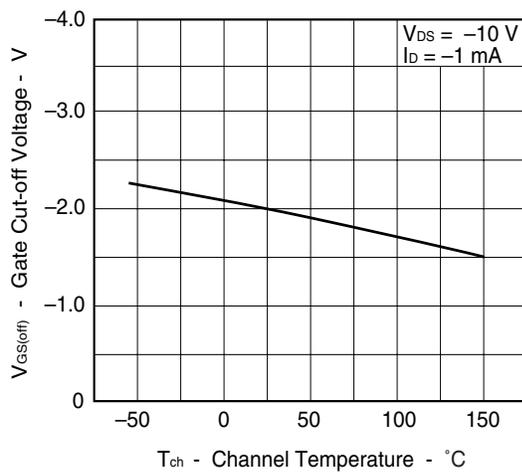
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

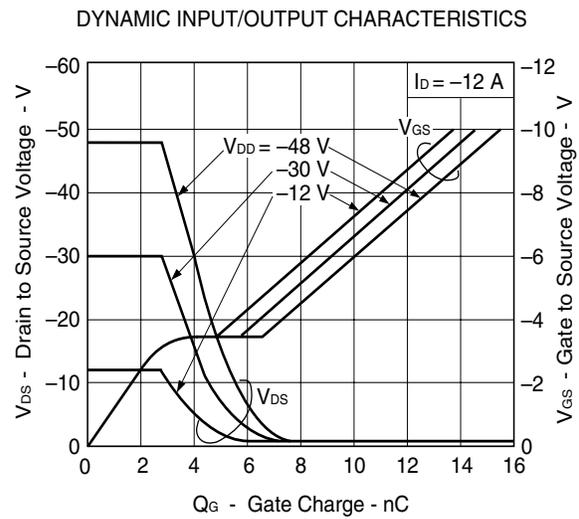
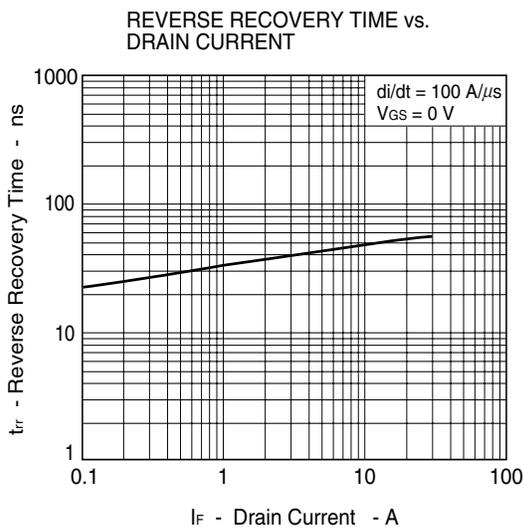
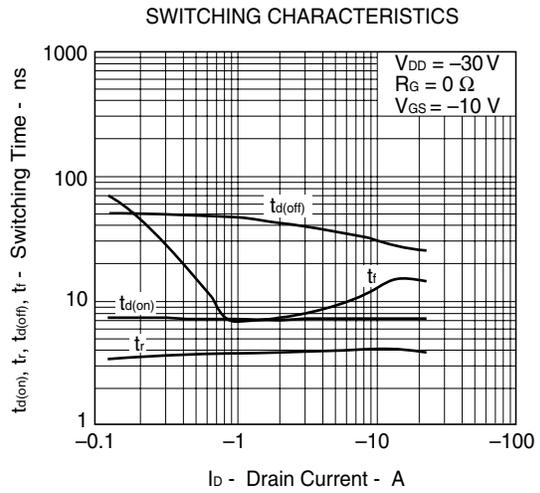
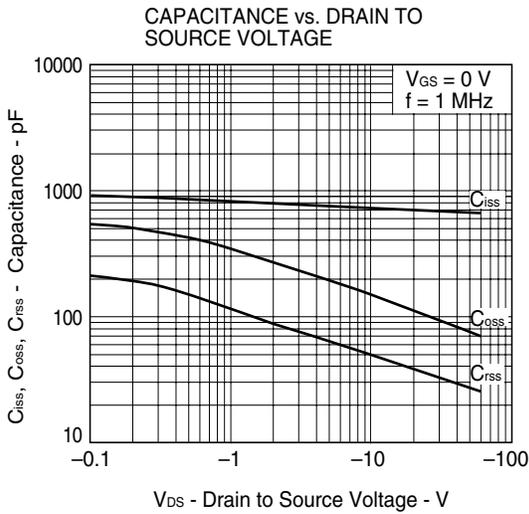
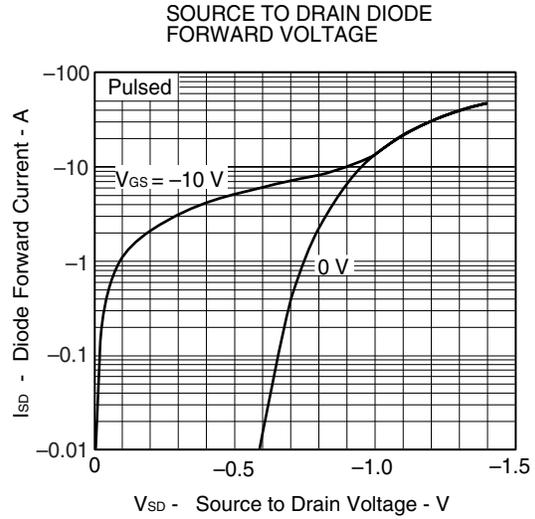
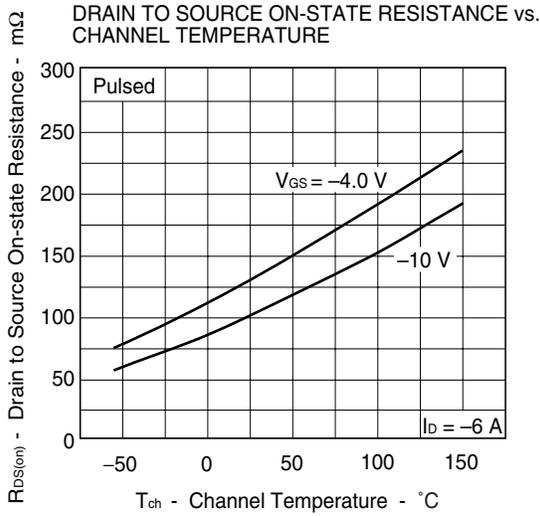


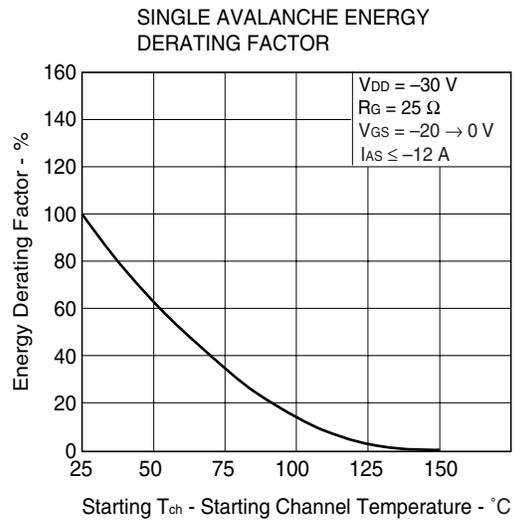
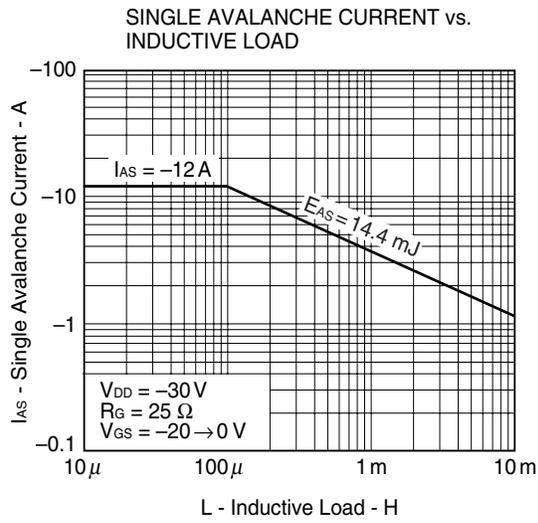
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

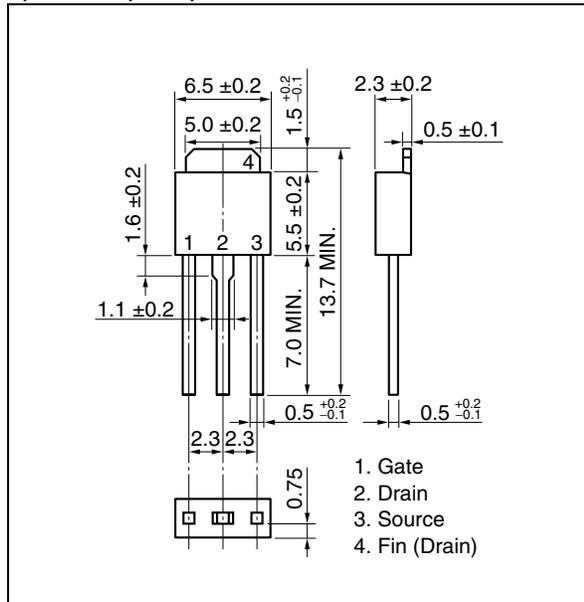




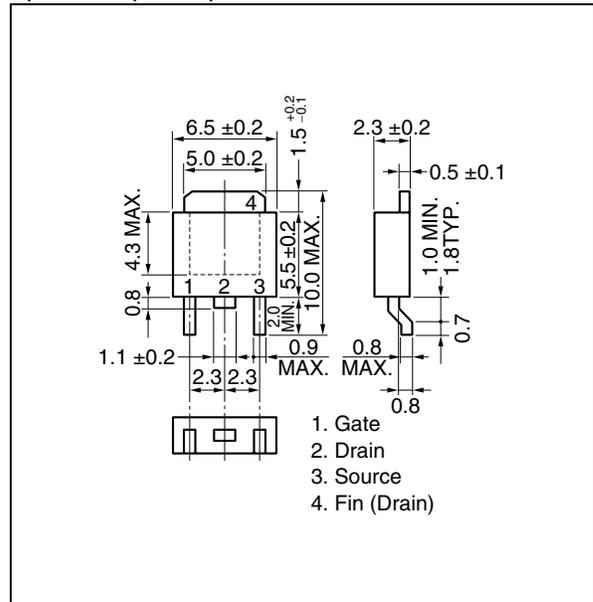


★ PACKAGE DRAWINGS (Unit: mm)

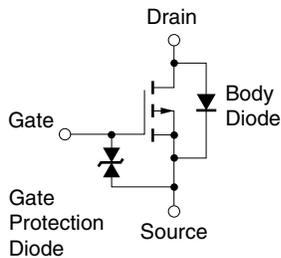
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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