74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Rev. 03 — 11 May 2004 **Product data sheet**

1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}D$, which also inhibits the triggering.
3. An internal connection from $n\overline{R}D$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\overline{R}D$ as shown in the function table.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 is identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

2. Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC123						
t_{PHL}, t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; C_L = 15 pF; V_{CC} = 5 V	-	26	-	ns
	propagation delay $n\overline{RD}$ to nQ, $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; C_L = 15 pF; V_{CC} = 5 V	-	20	-	ns
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per monostable	[1] [2]	-	54	-	pF
Type 74HCT123						
t_{PHL}, t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; C_L = 15 pF; V_{CC} = 5 V	-	26	-	ns
	propagation delay $n\overline{RD}$ to nQ, $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; C_L = 15 pF; V_{CC} = 5 V	-	23	-	ns
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per monostable	[1] [3]	-	56	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
D = duty factor in %;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
C_{EXT} = timing capacitance in pF;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

[2] For 74HC123 the condition is V_I = GND to V_{CC}.

[3] For 74HCT123 the condition is V_I = GND to V_{CC} – 1.5 V.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT123N	–40 °C to +125 °C			
74HC123D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT123D	–40 °C to +125 °C			

Table 2: Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HC123DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT123DB	–40 °C to +125 °C			
74HC123PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT123PW	–40 °C to +125 °C			

5. Functional diagram

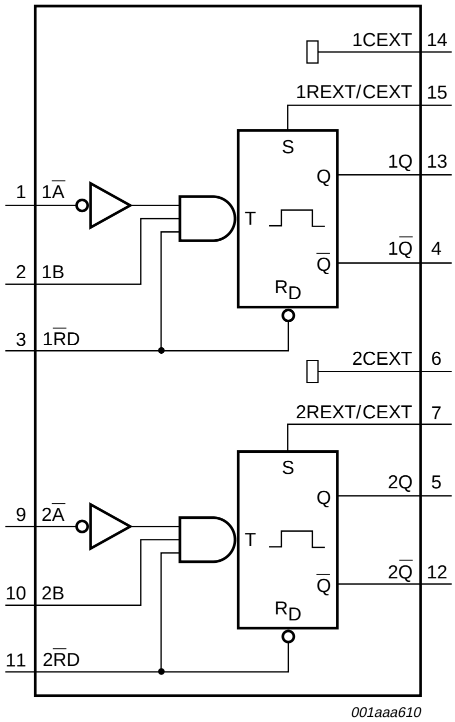


Fig 1. Functional diagram.

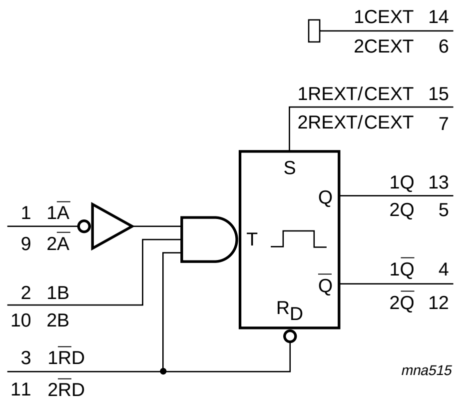


Fig 2. Logic symbol.

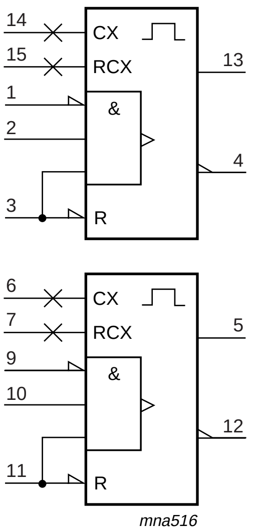


Fig 3. IEC logic symbol.

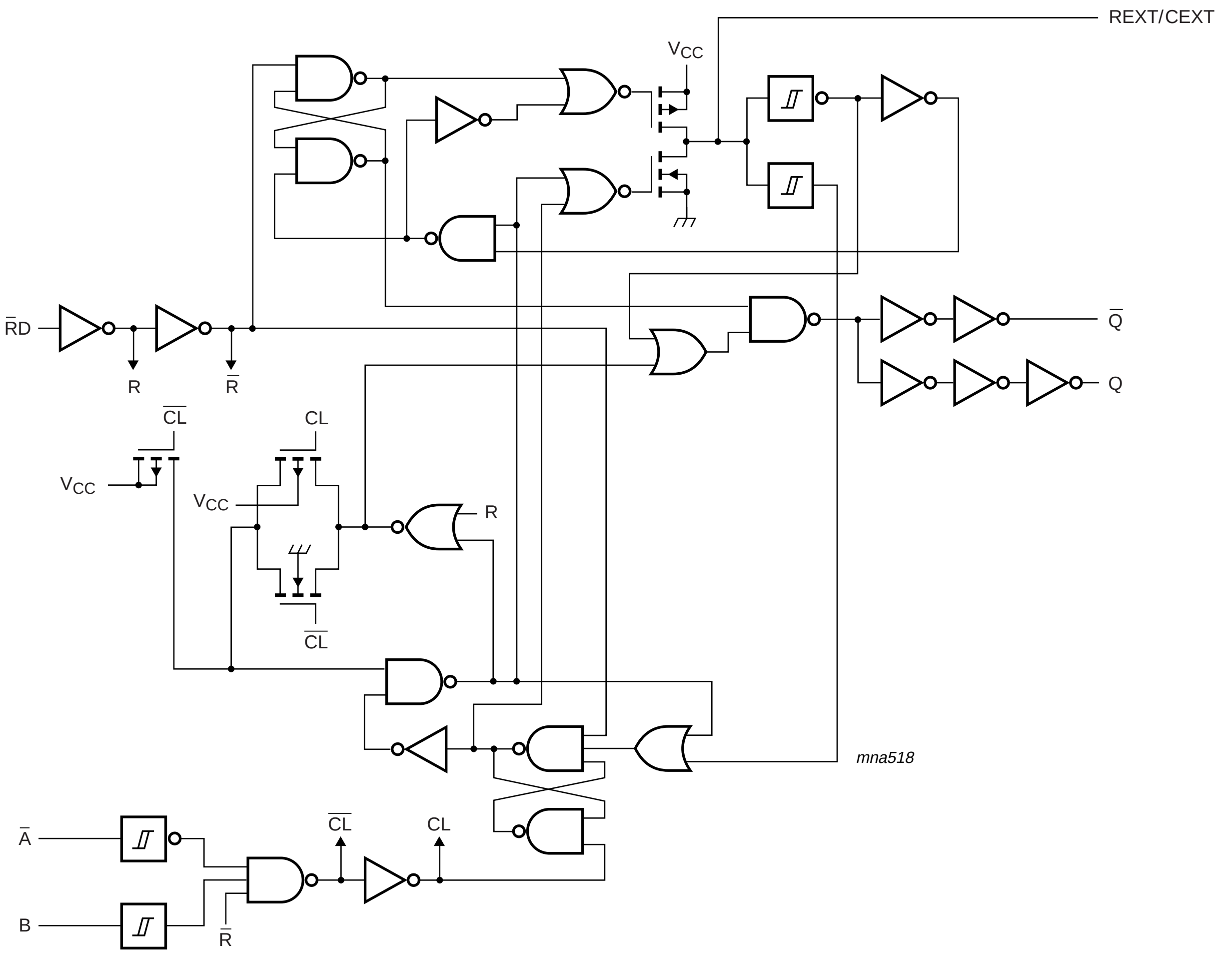


Fig 4. Logic diagram.

6. Pinning information

6.1 Pinning

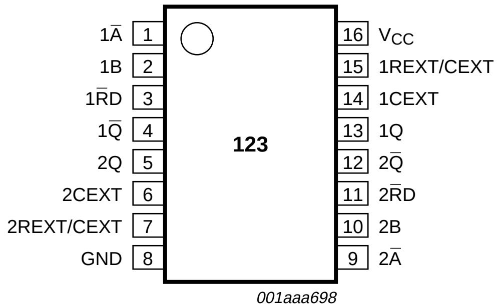


Fig 5. Pin configuration.

6.2 Pin description

Table 3: Pin description

Pin	Symbol	Description
1	1$\overline{A}$	trigger inputs (negative-edge triggered)
2	1B	trigger inputs (positive-edge triggered)
3	1$\overline{RD}$	direct reset LOW and trigger action at positive edge
4	1$\overline{Q}$	outputs (active LOW)
5	2Q	outputs (active HIGH)
6	2CEXT	external capacitor connection
7	2REXT/CEXT	external resistor and capacitor connection
8	GND	ground (0 V)
9	2$\overline{A}$	trigger inputs (negative-edge triggered)
10	2B	trigger inputs (positive-edge triggered)
11	2$\overline{RD}$	direct reset LOW and trigger action at positive edge
12	2$\overline{Q}$	outputs (active LOW)
13	1Q	outputs (active HIGH)
14	1CEXT	external capacitor connection
15	1REXT/CEXT	external resistor and capacitor connection
16	V_{CC}	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input			Output	
$n\overline{RD}$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L [2]	H [2]
X	X	L	L [2]	H [2]
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⊓ = one HIGH level output pulse
⊔ = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output source or sink current, except for pins nREXT/CEXT	$V_O = –0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	DIP16 package	[1]	-	750	mW
	SO16, SSOP16 and TSSOP16 packages	[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC123						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times for n$\overline{RD}$ input	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
T_{amb}	operating ambient temperature	see Section 10 and 11	–40	-	+125	°C
Type 74HCT123						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times for n$\overline{RD}$ input	V_{CC} = 4.5 V	-	6.0	500	ns
T_{amb}	operating ambient temperature	see Section 10 and 11	–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics type 74HC123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V

Table 7: Static characteristics type 74HC123 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	0	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	0	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	0	0.1	V
		$I_O = 4$ mA; $V_{CC} = 4.5$ V	-	0.15	0.26	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\ \mu A$; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4$ mA; $V_{CC} = 4.5$ V	3.84	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 4.5$ V	-	-	0.33	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	80	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V

Table 7: Static characteristics type 74HC123 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		$I_O = -20$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20$ µA; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160	µA

Table 8: Static characteristics type 74HCT123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ µA	4.4	4.5	-	V
		$I_O = -4$ mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ µA	-	0	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pins $n\overline{A}$, nB	-	35	125	µA
		pin $n\overline{RD}$	-	50	180	µA
C_I	input capacitance		-	3.5	-	pF
$T_{amb} = -40$ °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V

Table 8: Static characteristics type 74HCT123 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 2.1 V; other inputs $V_I = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
		pins $n\overline{A}$, nB	-	-	160	μA
		pin $n\overline{RD}$	-	-	225	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4 mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±10.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 2.1 V; other inputs $V_I = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
		pins $n\overline{A}$, nB	-	-	170	μA
		pin $n\overline{RD}$	-	-	245	μA

11. Dynamic characteristics

Table 9: Dynamic characteristics type 72HC123

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 2.0 V		-	83	255	ns
		V_{CC} = 4.5 V		-	30	51	ns
		V_{CC} = 6.0 V		-	24	43	ns
		C_L = 15 pF; V_{CC} = 5 V		-	26	-	ns
	propagation delay n$\overline{RD}$ to nQ or n$\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 2.0 V		-	66	215	ns
		V_{CC} = 4.5 V			24	43	
		V_{CC} = 6.0 V		-	19	37	ns
		C_L = 15 pF; V_{CC} = 5 V		-	20	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6					
		V_{CC} = 2.0 V		-	19	75	ns
		V_{CC} = 4.5 V		-	7	15	ns
		V_{CC} = 6.0 V		-	6	13	ns
t_W	trigger pulse width	n$\overline{A}$ = LOW; see Figure 7					
		V_{CC} = 2.0 V		100	8	-	ns
		V_{CC} = 4.5 V		20	3	-	ns
		V_{CC} = 6.0 V		17	2	-	ns
		nB = HIGH; see Figure 7					
		V_{CC} = 2.0 V		100	17	-	ns
		V_{CC} = 4.5 V		20	6	-	ns
		V_{CC} = 6.0 V		17	5	-	ns
	reset pulse width	n$\overline{RD}$ = LOW; see Figure 8					
		V_{CC} = 2.0 V		100	14	-	ns
		V_{CC} = 4.5 V		20	5	-	ns
		V_{CC} = 6.0 V		17	4	-	ns
	output pulse width	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; V_{CC} = 5.0 V; nQ = HIGH; n$\overline{Q}$ = LOW; see Figure 7 and 8		-	450	-	µs
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; nQ = HIGH; n$\overline{Q}$ = LOW; see Figure 7 and 8	[1]	-	75	-	ns
t_{rt}	retrigger time n$\overline{A}$, nB	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 7	[2] [3]	-	110	-	ns
R_{EXT}	external timing resistor	see Figure 10					
		V_{CC} = 2.0 V		10	-	1000	kΩ
		V_{CC} = 5.0 V		2	-	1000	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 10	[3]		no limits		pF

Table 9: Dynamic characteristics type 72HC123 *…continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{PD}	power dissipation capacitance per monostable	[4] [5]	-	54	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6				
		V_{CC} = 2.0 V	-	-	320	ns
		V_{CC} = 4.5 V	-	-	64	ns
		V_{CC} = 6.0 V	-	-	54	ns
	propagation delay n$\overline{RD}$ to nQ or n$\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6				
		V_{CC} = 2.0 V	-	-	270	ns
		V_{CC} = 4.5 V		-	54	
		V_{CC} = 6.0 V	-	-	46	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	trigger pulse width	n$\overline{A}$ = LOW; see Figure 7				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
		nB = HIGH; see Figure 7				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
	reset pulse width	n$\overline{RD}$ = LOW; see Figure 8				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6				
		V_{CC} = 2.0 V	-	-	385	ns
		V_{CC} = 4.5 V	-	-	77	ns
		V_{CC} = 6.0 V	-	-	65	ns
	propagation delay n$\overline{RD}$ to nQ or n$\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6				
		V_{CC} = 2.0 V	-	-	325	ns
		V_{CC} = 4.5 V		-	65	
		V_{CC} = 6.0 V	-	-	55	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns

Table 9: Dynamic characteristics type 72HC123 *…continued*

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; unless otherwise specified; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	trigger pulse width	$n\overline{A}$ = LOW; see Figure 7				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns
		nB = HIGH; see Figure 7				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns
	reset pulse width	$n\overline{RD}$ = LOW; see Figure 8				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns

[1] For other R_{EXT} and C_{EXT} combinations see Figure 10. If $C_{EXT} > 10$ nF, the next formula is valid:
$t_W = K \times R_{EXT} \times C_{EXT}$, where:
t_W = typical output pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF;
K = constant = 0.45 for $V_{CC} = 5.0$ V and 0.48 for $V_{CC} = 2.0$ V.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} >10 pF, the next formula (at $V_{CC} = 5.0$ V) for the set-up time of a retrigger pulse is valid:
$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:
t_{rt} = retrigger time in ns;
C_{EXT} = external capacitor in pF;
R_{EXT} = external resistor in kΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[3] When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
D = duty factor in %;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
C_{EXT} = timing capacitance in pF;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

[5] The condition is V_I = GND to V_{CC}.

Table 10: Dynamic characteristics type 72HCT123

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 4.5 V		-	30	51	ns
		C_L = 15 pF; V_{CC} = 5 V		-	26	-	ns
	propagation delay $n\overline{RD}$ to nQ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 4.5 V		-	27	46	ns
		C_L = 15 pF; V_{CC} = 5 V		-	23	-	ns
t_{PLH}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to nQ	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 4.5 V		-	28	51	ns
		C_L = 15 pF; V_{CC} = 5 V		-	26	-	ns
	propagation delay $n\overline{RD}$ to $n\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 6					
		V_{CC} = 4.5 V		-	23	46	ns
		C_L = 15 pF; V_{CC} = 5 V		-	23	-	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 6		-	7	15	ns
t_W	trigger pulse width	$n\overline{A}$ = LOW; V_{CC} = 4.5 V; see Figure 7		20	3	-	ns
		nB = HIGH; V_{CC} = 4.5 V; see Figure 7		20	5	-	ns
	reset pulse width	$n\overline{RD}$ = LOW; V_{CC} = 4.5 V; see Figure 8		20	7	-	ns
	output pulse width	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; V_{CC} = 5.0 V; nQ = HIGH; $n\overline{Q}$ = LOW; see Figure 7 and 8		-	450	-	µs
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; nQ = HIGH; $n\overline{Q}$ = LOW; see Figure 7 and 8	[1]	-	75	-	ns
t_{rt}	retrigger time $n\overline{A}$, nB	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 7	[2] [3]	-	110	-	ns
R_{EXT}	external timing resistor	V_{CC} = 5.0 V; see Figure 10		2	-	1000	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 10	[3]		no limits		pF
C_{PD}	power dissipation capacitance per monostable		[4] [5]	-	56	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6		-	-	64	ns
	propagation delay $n\overline{RD}$ to nQ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6		-	-	58	ns
t_{PLH}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to nQ	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6		-	-	64	ns
	propagation delay $n\overline{RD}$ to $n\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6		-	-	58	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V		-	-	19	ns
t_W	trigger pulse width	$n\overline{A}$ = LOW; V_{CC} = 4.5 V; see Figure 7		25	-	-	ns
		nB = HIGH; V_{CC} = 4.5 V; see Figure 7		25	-	-	ns
	reset pulse width	$n\overline{RD}$ = LOW; V_{CC} = 4.5 V; see Figure 8		25	-	-	ns

Table 10: Dynamic characteristics type 72HCT123 *…continued*

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; unless otherwise specified; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to $n\overline{Q}$	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6	-	-	77	ns
	propagation delay $n\overline{RD}$ to nQ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6	-	-	69	ns
t_{PLH}	propagation delay $n\overline{RD}$, $n\overline{A}$, nB to nQ	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6	-	-	77	ns
	propagation delay $n\overline{RD}$ to $n\overline{Q}$ (reset)	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 4.5 V; see Figure 6	-	-	69	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V	-	-	22	ns
t_W	trigger pulse width	$n\overline{A}$ = LOW; V_{CC} = 4.5 V; see Figure 7	30	-	-	ns
		nB = HIGH; V_{CC} = 4.5 V; see Figure 7	30	-	-	ns
	reset pulse width	$n\overline{RD}$ = LOW; V_{CC} = 4.5 V; see Figure 8	30	-	-	ns

[1] For other R_{EXT} and C_{EXT} combinations see Figure 10. If C_{EXT} > 10 nF, the next formula is valid:

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = constant = 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} >10 pF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:

t_{rt} = typical retrigger time in ns;

C_{EXT} = external capacitor in pF;

R_{EXT} = external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[3] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

D = duty factor in %;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

C_{EXT} = timing capacitance in pF;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

[5] The condition is V_I = GND to V_{CC} − 1.5 V.

12. Waveforms

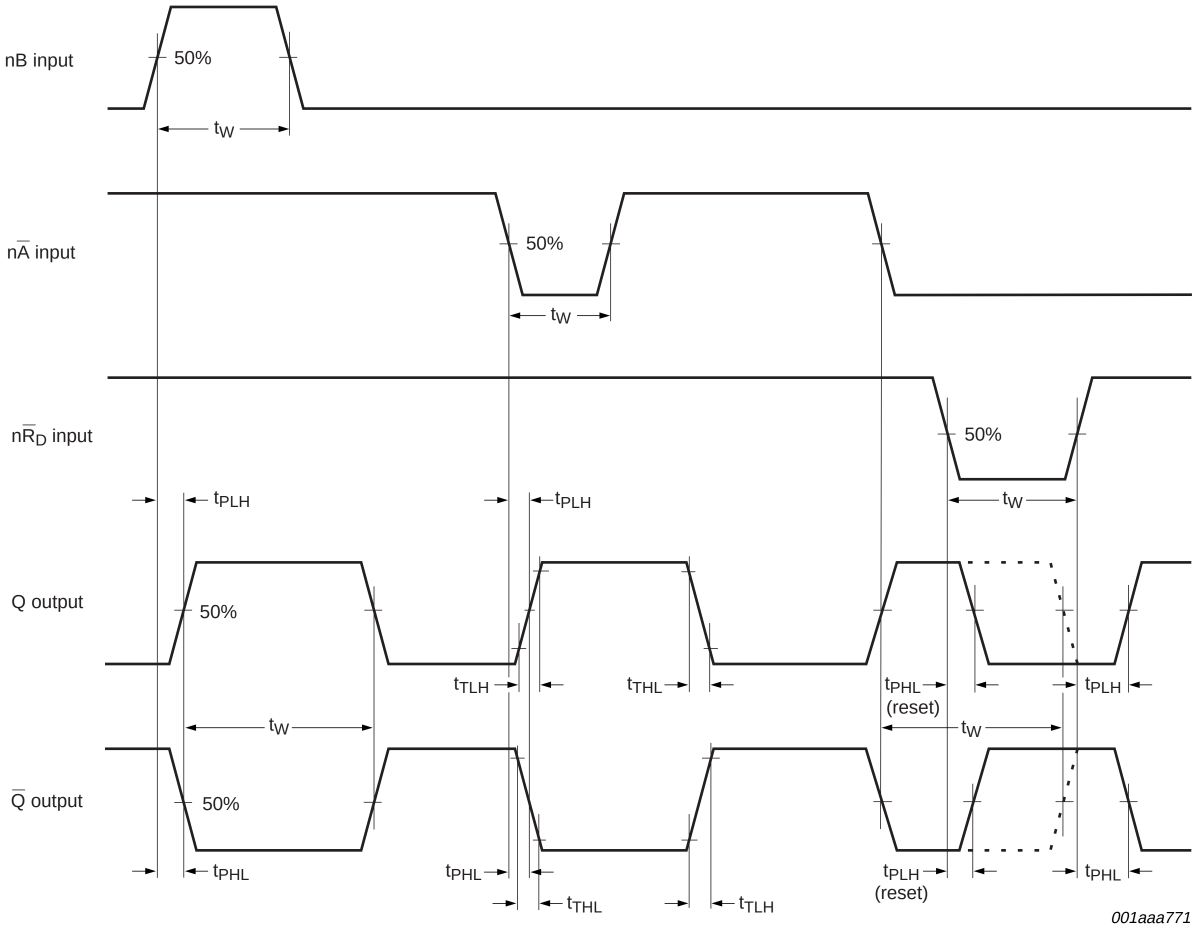
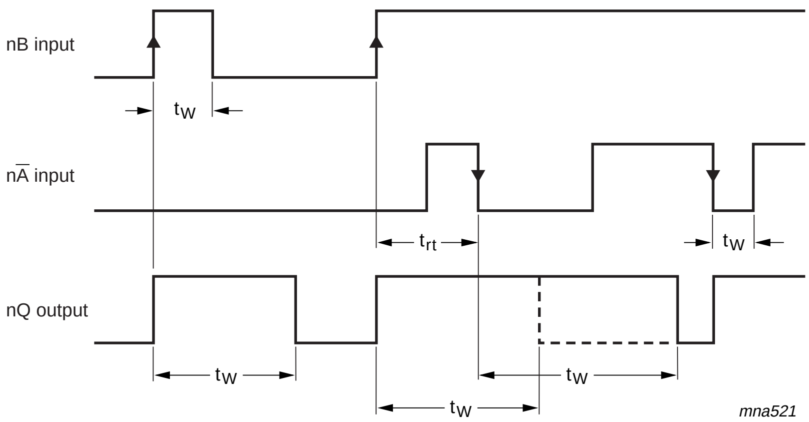
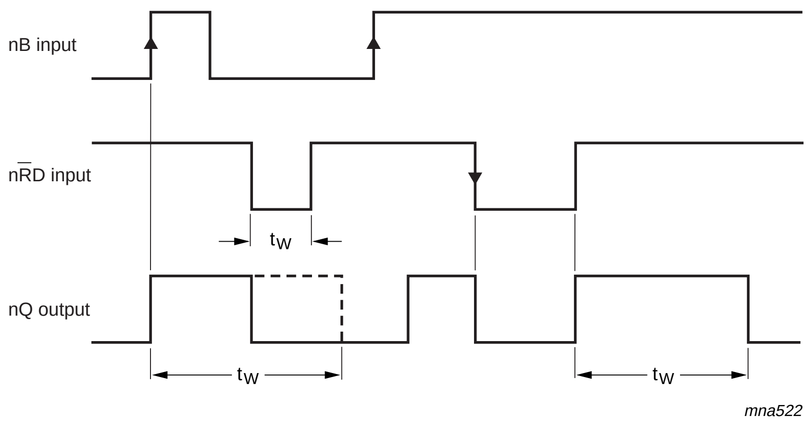


Fig 6. Propagation delays from inputs (n$\overline{A}$, nB, n$\overline{RD}$) to outputs (nQ, n$\overline{Q}$) and output transition times.



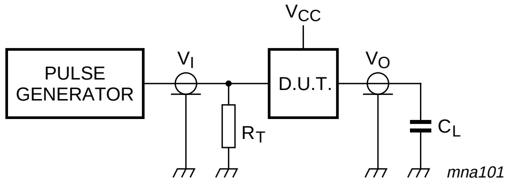
n$\overline{RD}$ = HIGH

Fig 7. Output pulse control using retrigger pulse.



nA = LOW

Fig 8. Output pulse control using reset input nRD.

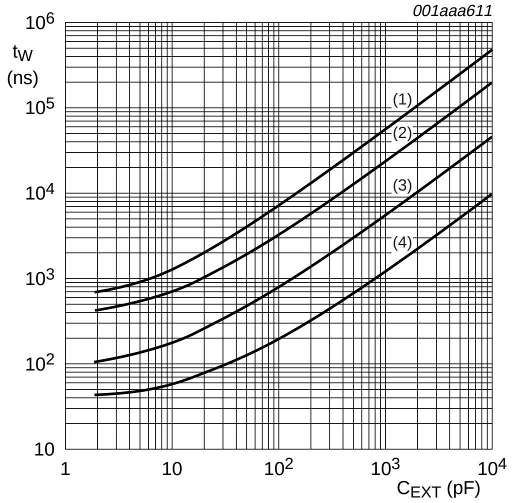


Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance (See Section 11 for the value).

Fig 9. Load circuitry for switching times.



V_{CC} = 5.0 V; T_{amb} = 25 °C.

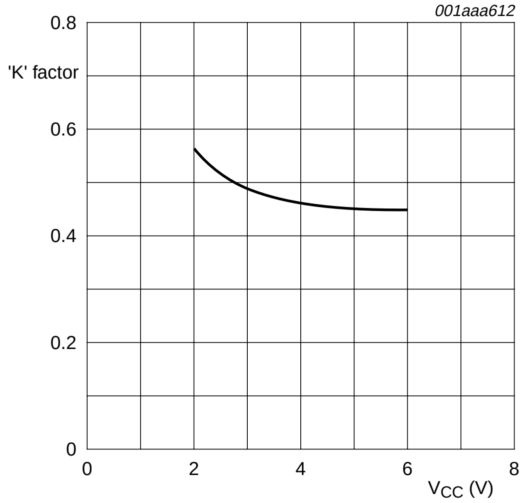
(1) R_{EXT} = 100 kΩ

(2) R_{EXT} = 50 kΩ

(3) R_{EXT} = 10 kΩ

(4) R_{EXT} = 2 kΩ

Fig 10. Typical output pulse width as a function of the external capacitor value.



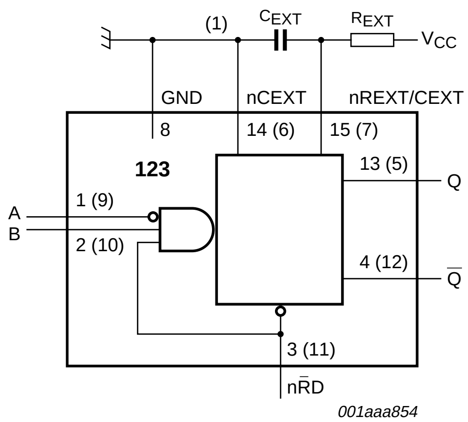
C_X = 10 nF; R_X = 10 kΩ to 100 kΩ

Fig 11. 74HCT123 typical 'K' factor as function of V_{CC}.

13. Application information

13.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



(1) For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

Fig 12. Timing component connections.

13.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the circuit shown in Figure 13.

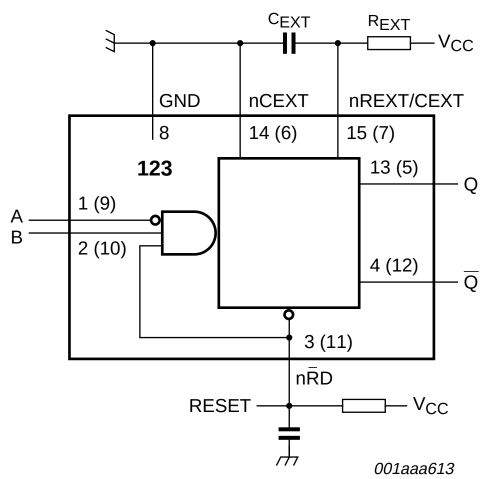


Fig 13. Power-up output pulse elimination circuit.

13.3 Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 14.

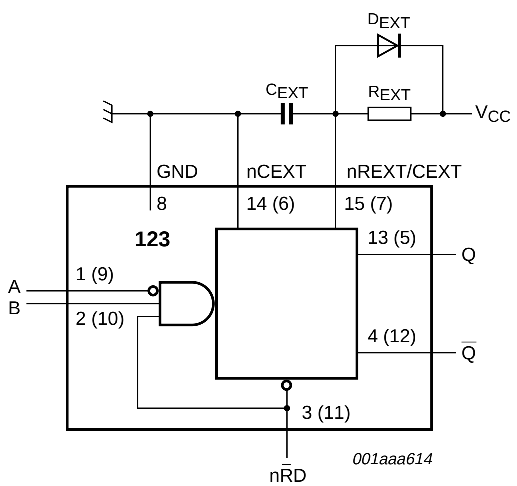
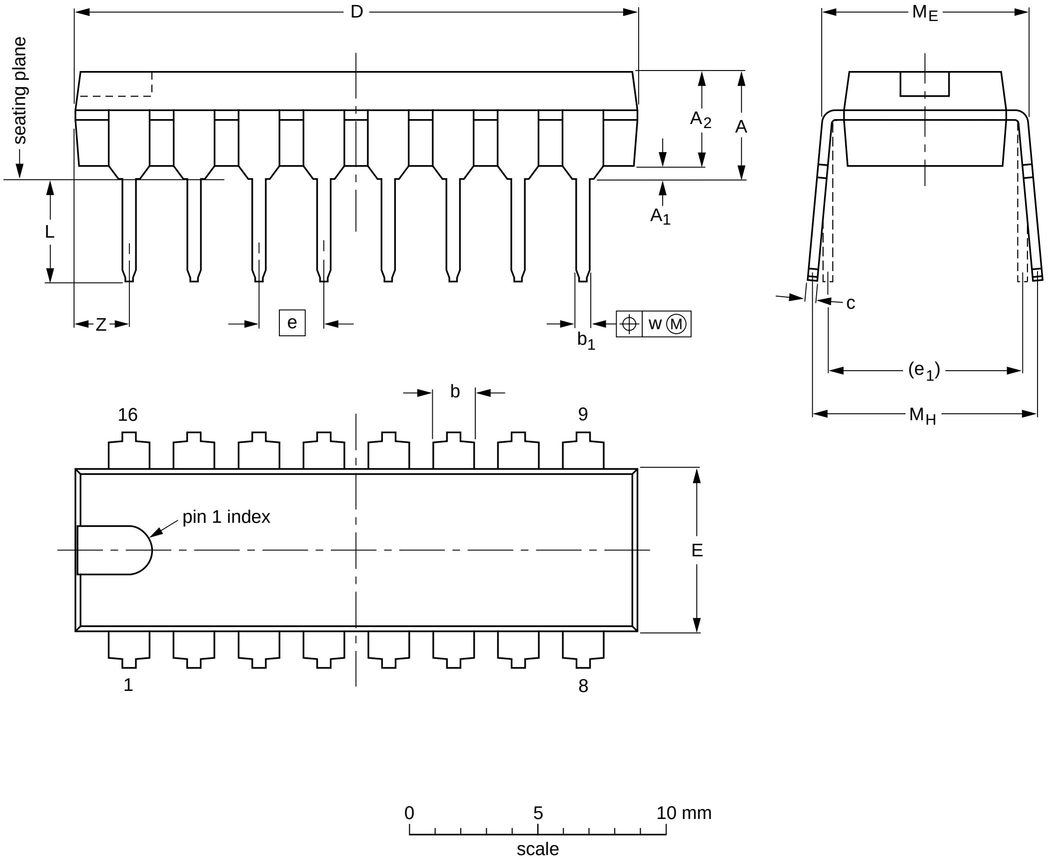


Fig 14. Power-down protection circuit.

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

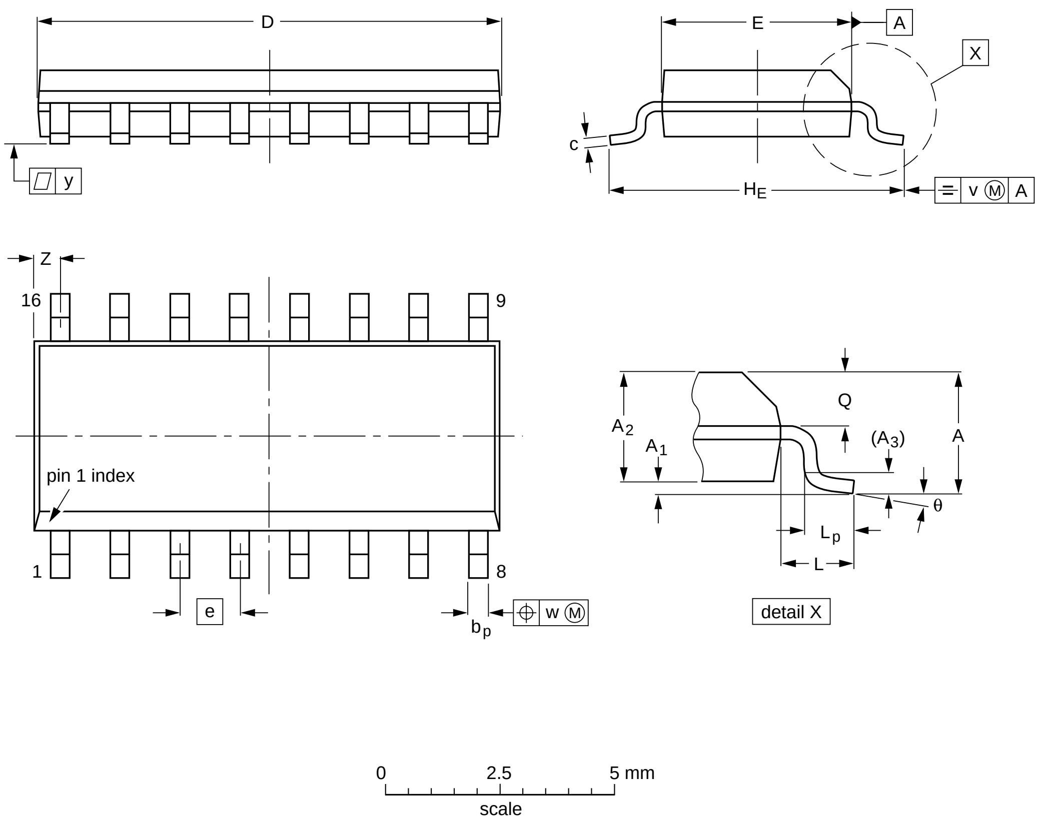
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 15. Package outline DIP16.

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

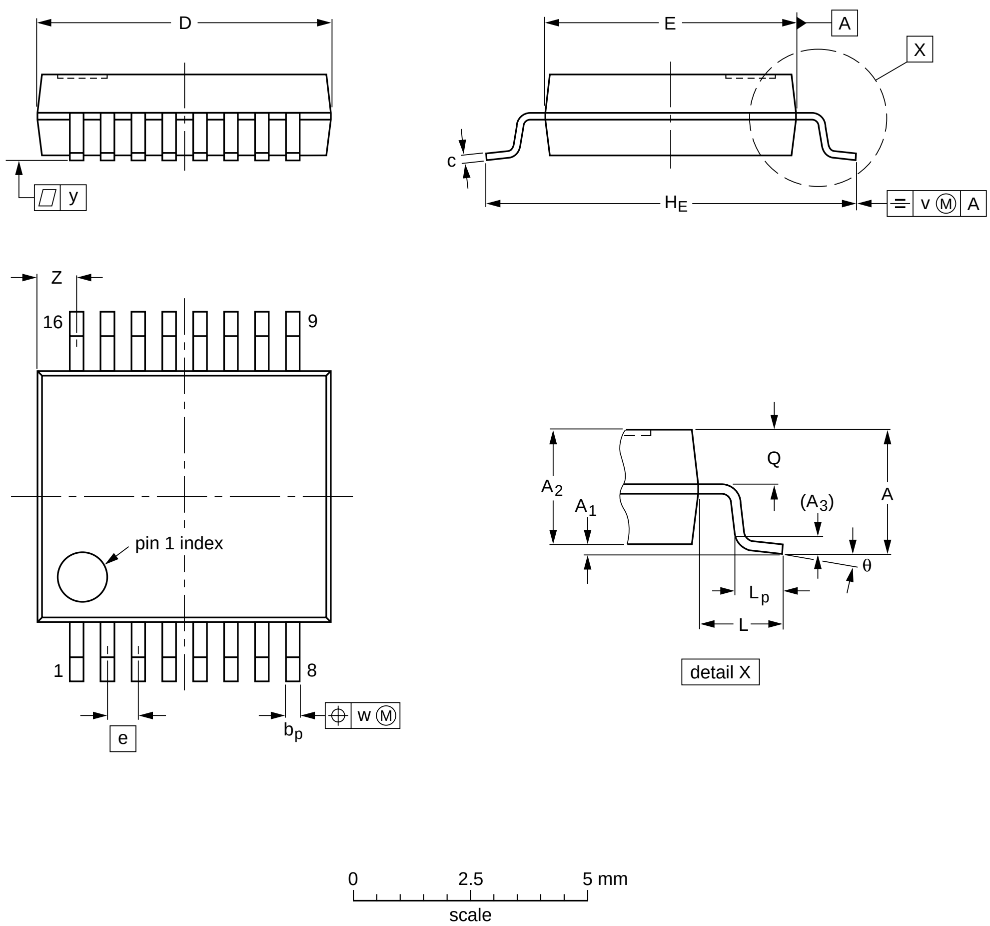
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SO16.

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

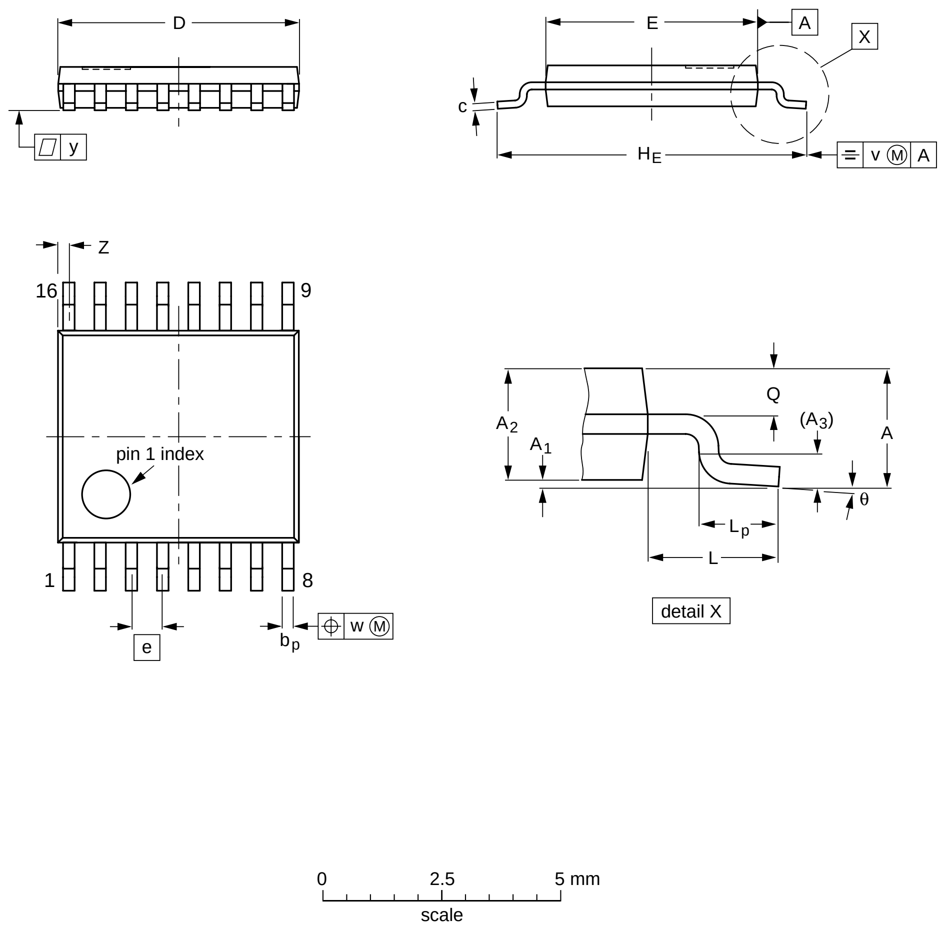
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SSOP16.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline TSSOP16.

15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74HC_HCT123_3	20040511	Product data	-	9397 750 13024	74HC_HCT123_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Section 2 on page 1: ESD clause added • Section 8 on page 6, Section 9 on page 7, and Section 10 on page 7: These sections replace references to family specifications • Table note 1 on page 13: Changed ‘K’ factor from 0.55 to 0.45 • Table note 1 on page 15: Changed ‘K’ factor from 0.55 to 0.45				
74HCHCT123_2	19980708	Product specification	-	-	74HC_HCT123_1

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

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20. Contents

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