ADC0800

8-Bit A/D Converter

Literature Number: SNAS562

National Semiconductor

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ADC0800 8-Bit A/D Converter

General Description

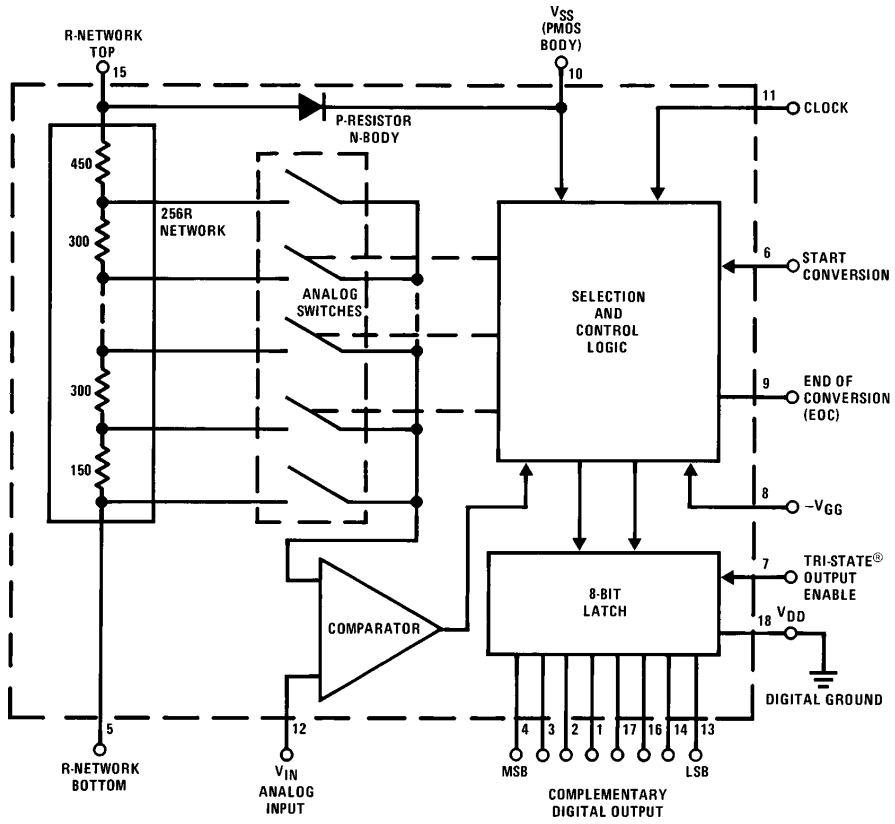
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — $T_C = 50\ \mu s$
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



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(00000000 = + full-scale)

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	$V_{SS}-22V$
Supply Voltage (V_{GG})	$V_{SS}-22V$
Voltage at Any Input	$V_{SS}+0.3V$ to $V_{SS}-22V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	875 mW
ESD Susceptibility (Note 4)	500V
Storage Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0800PD	$-55°C \le T_A \le +125°C$
ADC0800PCD	$0°C \le T_A \le +70°C$

Electrical Characteristics

These specifications apply for $V_{SS}=5.0\ V_{DC}$, $V_{GG}=-12.0\ V_{DC}$, $V_{DD}=0\ V_{DC}$, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}=5.000\ V_{DC}$ and $V_{R\text{-}NETWORK\ BOTTOM}=-5.000\ V_{DC}$), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to $V_{R\text{-}NETWORK\ BOTTOM} = -5\ V_{DC}$. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

Parameter	Conditions	Min	Typ	Max	Units
Non-Linearity	$T_A=25°C$, (Note 8) Over Temperature, (Note 8)			±1 ±2	LSB LSB
Differential Non-Linearity				±½	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 9)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 9)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	$V_{SS}-1.0$		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		$V_{SS}-4.2$	V
Logical Input Leakage	$T_A=25°C$, All Inputs, $V_{IL}=V_{SS}-10V$			1	μA
Logical "1" Output Voltage	All Outputs, $I_{OH}=100\ \mu A$	2.4			V
Logical "0" Output Voltage	All Outputs, $I_{OL}=1.6$ mA			0.4	V
Disabled Output Leakage	$T_A=25°C$, All Outputs, $V_{OL}=V_{SS}$@10V			2	μA
Clock Frequency	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	50 100		800 500	kHz kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 10)	1		3½	Clock Periods
Power Supply Current	$T_A=25°C$			20	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the ADC0800PD and ADC0800PCD when board mounted is 66°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

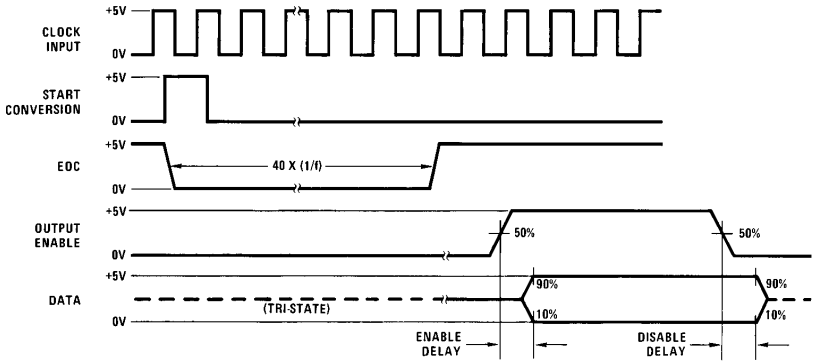
Note 7: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Non-linearity specifications are based on best straight line.

Note 9: Guaranteed by design only.

Note 10: Start conversion pulse duration greater than 3½ clock periods will cause conversion errors.

Timing Diagram



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Data is complementary binary (full scale is all ''0's'' output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and ¾ V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time in the latches. The data outputs are activated when the Output Enable is high, and in TRI-STATE when Output Enable is low. The Enable Delay time is approximately 200 ns. Each conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. $V_{REF} = 10.00V$ with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, applied to the top of the R-network (pin 15), must not exceed V_{SS}, to prevent forward biasing the on-chip parasitic silicon diodes that exist between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp that is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage that is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{GG}$ supply voltage to ensure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_S \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pickup due to unavoidable series lead inductance.
For $5k < R_S \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_S > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to ensure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical ''1'' input voltage swing for the Clock, Start Conversion and Output Enable should be ($V_{SS} - 1.0V$).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse that occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses that occur during this last 4 clock period interval may be ignored (see *Figure 1* and *2* for high speed operation). This is a problem only for high conversion rates and keeping the number of conversions per second less than $f_{CLOCK}/44$ automatically guarantees proper operation. For example, for an 800 kHz clock, approximately 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are $V_{SS} = +5V$, $V_{GG} = -12V$ and $V_{DD} = 0V$. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to V_{SS}—V_{GG}. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse that may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, to continuously convert for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

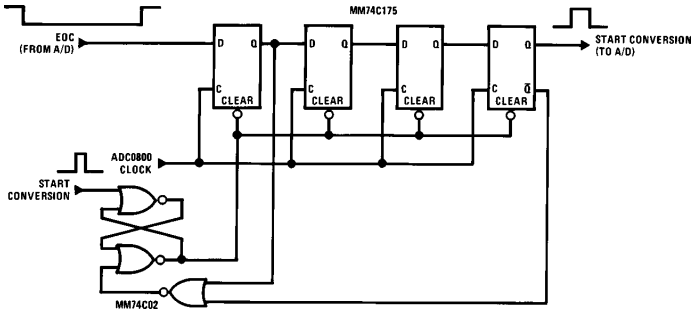

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FIGURE 1. Delaying an Asynchronous Start Pulse

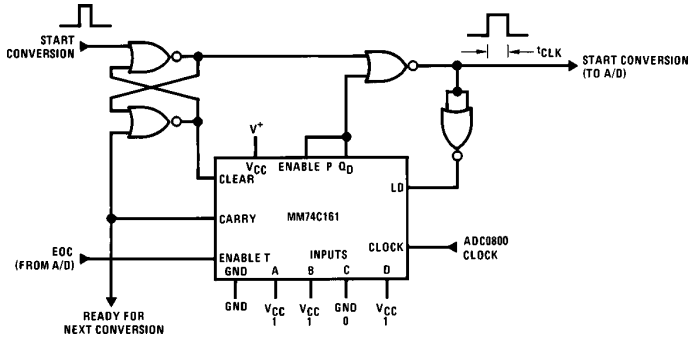

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FIGURE 2. A/D Control Logic

Application Hints (Continued)

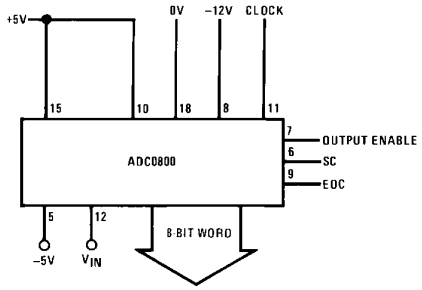
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is ½ LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 ½ LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within ±2 LSB for the ADC0800 without adjustment. In most cases, adjustment can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

General Connection



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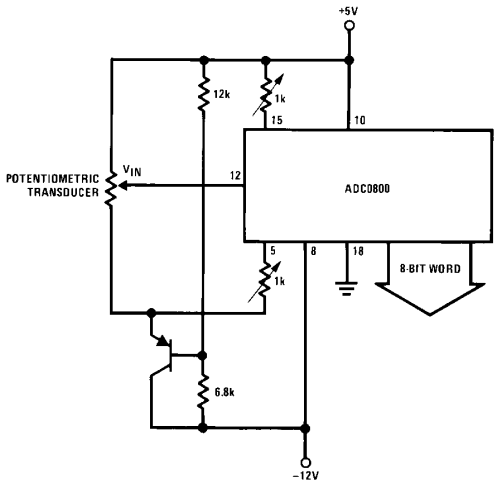
Ratiometric Input Signal with Tracking Reference



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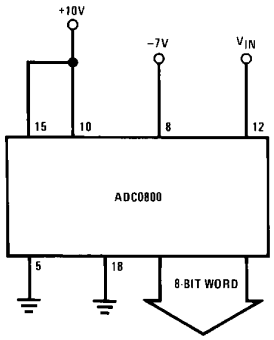
Hi-Voltage CMOS Output Levels



0V to 10V V_{IN} range
0V to 10V output levels

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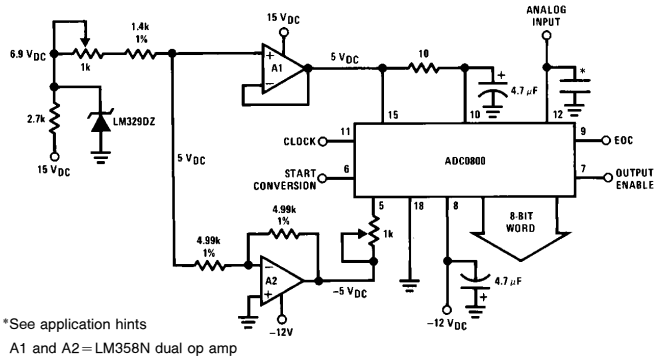
Typical Applications (Continued)

$V_{REF} = 10\ V_{DC}$ With TTL Logic Levels



*See application hints

A1 and A2 = LM358N dual op amp

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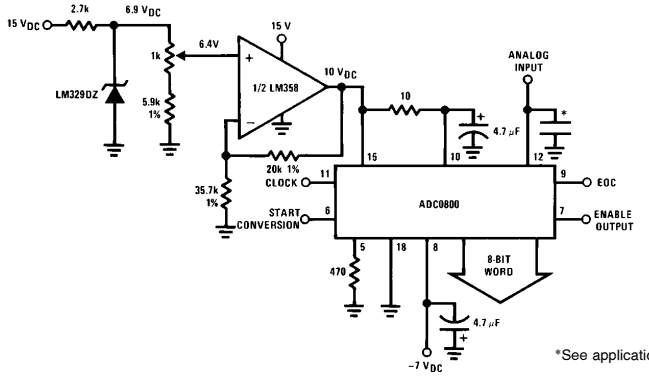
$V_{REF} = 10\ V_{DC}$ With 10V CMOS Logic Levels



*See application hints

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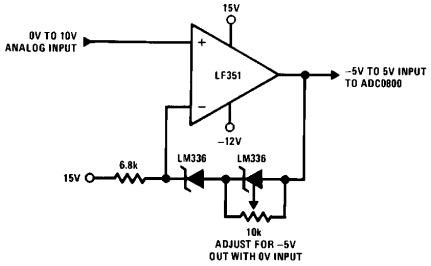
Input Level Shifting



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- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 3*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of ½ LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input that is 1½ LSB less than the reference (10.240−0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 4*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

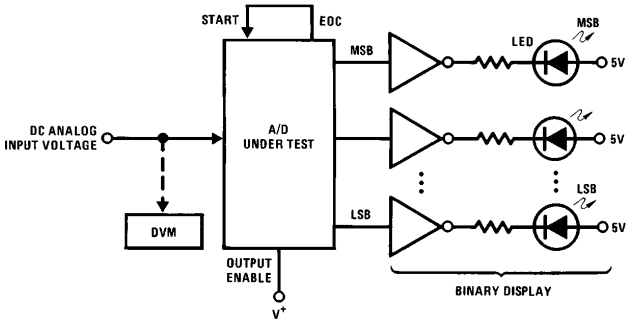

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FIGURE 3. Basic A/D Tester

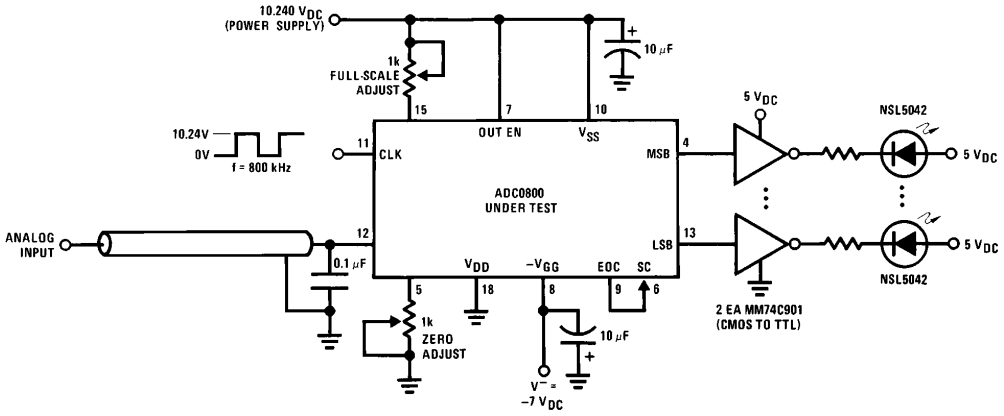

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FIGURE 4. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: ''Input Voltage Value with a 10.240 V_{REF}'' of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of ''1011 0110'' or ''B6'' (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±½ LSB (±20 mV), the ''quantization uncertainty'' of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 5* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
					MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1	1	1	1	15/16	15/256	9.600	0.600
E	1	1	1	0	7/8	7/128	8.960	0.560
D	1	1	0	1	13/16	13/256	8.320	0.520
C	1	1	0	0	3/4	3/64	7.680	0.480
B	1	0	1	1	11/16	11/256	7.040	0.440
A	1	0	1	0	5/8	5/128	6.400	0.400
9	1	0	0	1	9/16	9/256	5.760	0.360
8	1	0	0	0	1/2	1/32	5.120	0.320
7	0	1	1	1	7/16	7/256	4.480	0.280
6	0	1	1	0	3/8	3/128	3.840	0.240
5	0	1	0	1	5/16	5/256	3.200	0.200
4	0	1	0	0	1/4	1/64	2.560	0.160
3	0	0	1	1	3/16	3/256	1.920	0.120
2	0	0	1	0	1/8	1/128	1.280	0.080
1	0	0	0	1	1/16	1/256	0.640	0.040
0	0	0	0	0			0	0

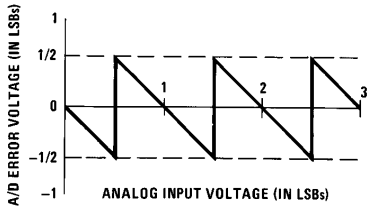

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FIGURE 5. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 6*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, ''A–C''.

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 7* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

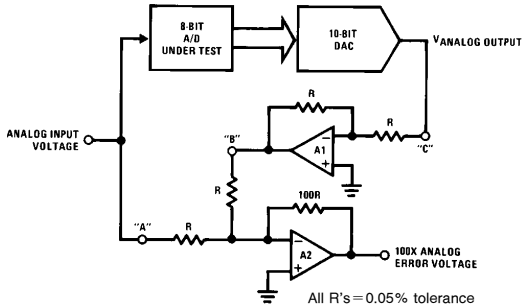

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FIGURE 6. A/D Tester with Analog Error Output

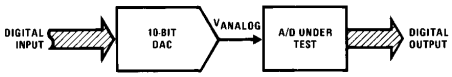

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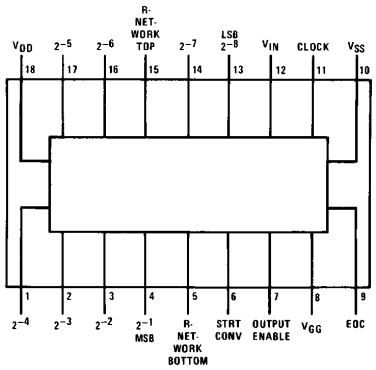
FIGURE 7. Basic ''Digital'' A/D Tester

Connection Diagram

Dual-In-Line Package



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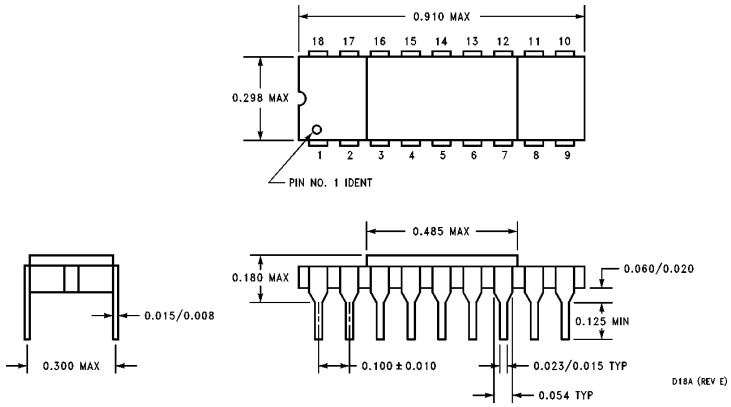
Top View

Order Number ADC0800PD
or ADC0800PCD
See NS Package Number D18A

Physical Dimensions inches (millimeters)



Hermetic Dual-In-Line Package (D)
Order Number ADC0800PD or ADC0800PCD
NS Package Number D18A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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