Improved Quad CMOS Analog Switches

FEATURES

- $\pm$22-V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance—$r_{DS(on)}$: 50 Ω
- Low Leakage—$I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching—t_{ON}: 120 ns
- Low Charge Injection—Q: 1 pC

BENEFITS

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG211/212
- Space Savings (TSSOP)

APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

DESCRIPTION

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

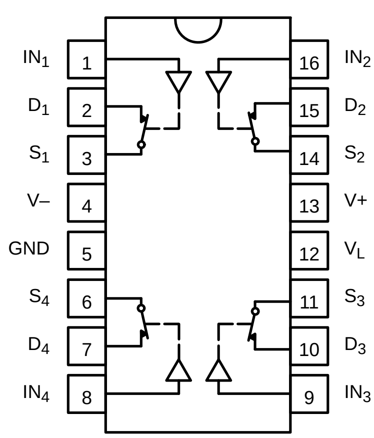
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG211B and DG212B can handle up to $\pm$22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG211B
Dual-In-Line, SOIC and TSSOP



Top View

TRUTH TABLE		
Logic	**DG211B**	**DG212B**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
–40 to 85°C	16-Pin Plastic DIP	DG211BDJ
		DG212BDJ
	16-Pin Narrow SOIC	DG211BDY
		DG212BDY
	16-Pin TSSOP	DG211BDQ
		DG212BDQ

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–
V+ . . . . 44 V
GND . . . . 25 V
Digital Inputs[a] V_S, V_D . . . . (V–) –2 V to (V+) +2 V or 30 mA, whichever occurs first
Current, Any Terminal . . . . 30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max) . . . . 100 mA
Storage Temperature . . . . –65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] . . . . 470 mW
16-Pin Narrow SOIC and TSSOP[d] . . . . 640 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

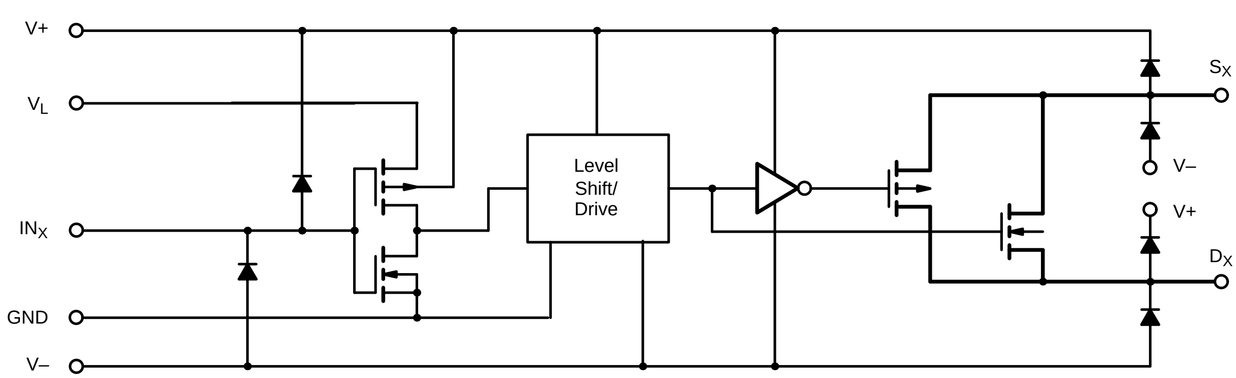


FIGURE 1.

SPECIFICATIONS

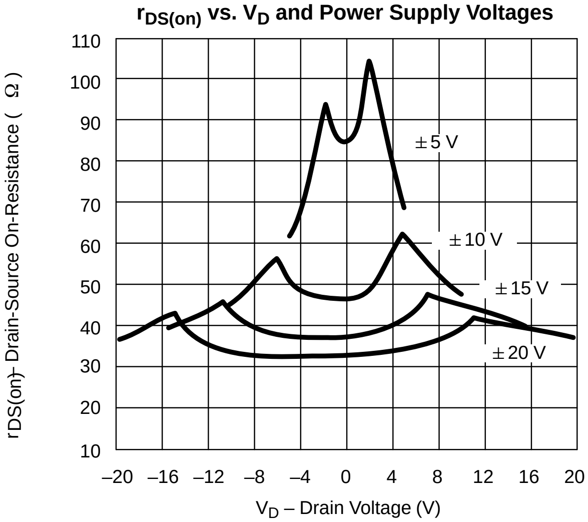
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room Full		45	85 100	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		2		Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	–0.5 –5	±0.01	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	–0.5 –5	±0.01	0.5 5	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±14 V	Room Full	–0.5 –10	±0.02	0.5 10	nA
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	V
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full	–1		1	µA
Input Capacitance	C_{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S =10 V See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	ns
Charge Injection	Q	C_L = 1000 pF, V_g= 0 V, R_g = 0 Ω	Room		1		pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		5		pF
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room		16		pF
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω V_S = 1 V_{RMS}, f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		95		dB
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I–		Room Full	–10 –50			µA
Logic Supply Current	I_L		Room Full			10 50	µA
Power Supply Range for Continuous Operation	V_{OP}		Full	±4.5		±22	V

SPECIFICATIONS FOR SINGLE SUPPLY							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 8 V See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection	Q	C_L = 1 nF, V_{gen}= 6 V, R_{gen} = 0 Ω	Room		4		pC
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I–		Room Full	–10 –50			
Logic Supply Current	I_L		Room Full			10 50	
Power Supply Range for Continuous Operation	V_{OP}		Full	+4.5		+25	V

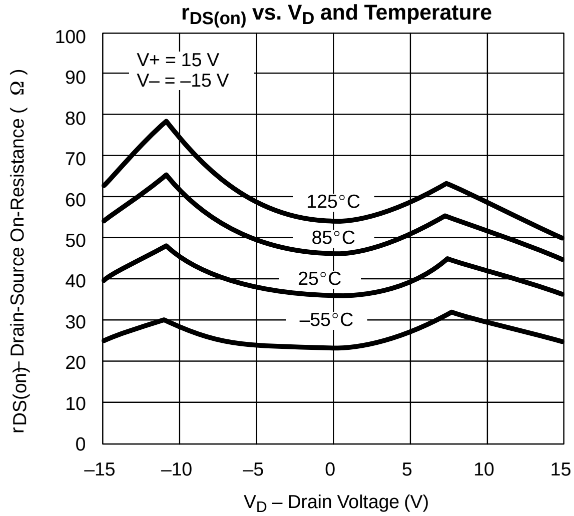
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

$r_{DS(on)}$ vs. V_D and Power Supply Voltages



$r_{DS(on)}$ vs. V_D and Temperature



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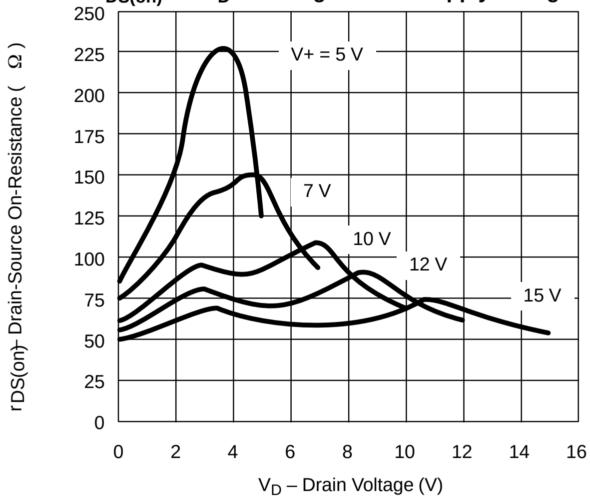
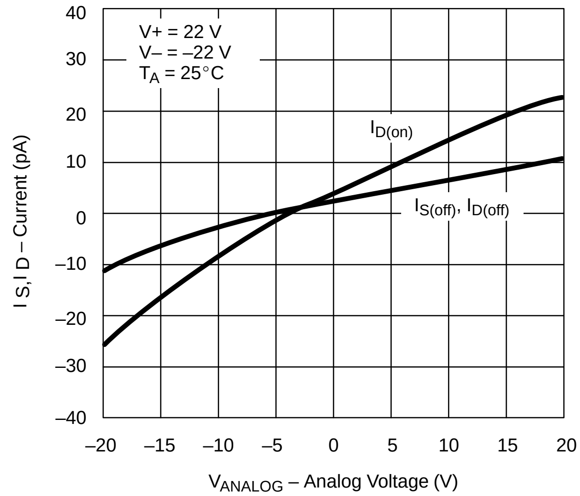
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

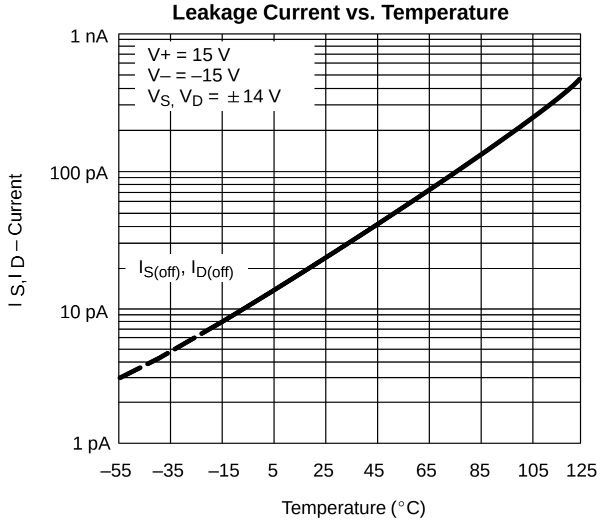
$r_{DS(on)}$ vs. V_D and Single Power Supply Voltages



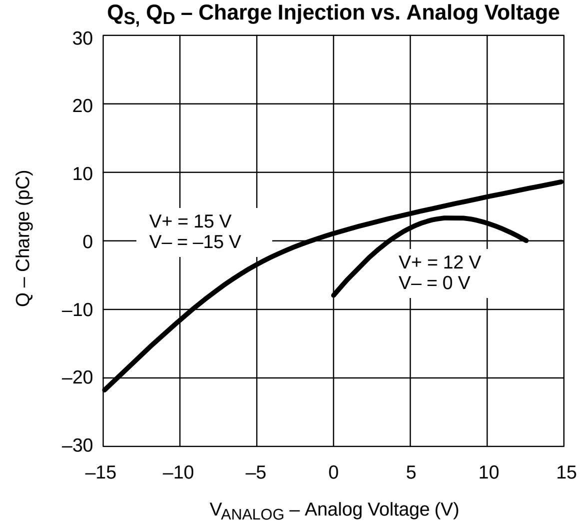
Leakage Currents vs. Analog Voltage



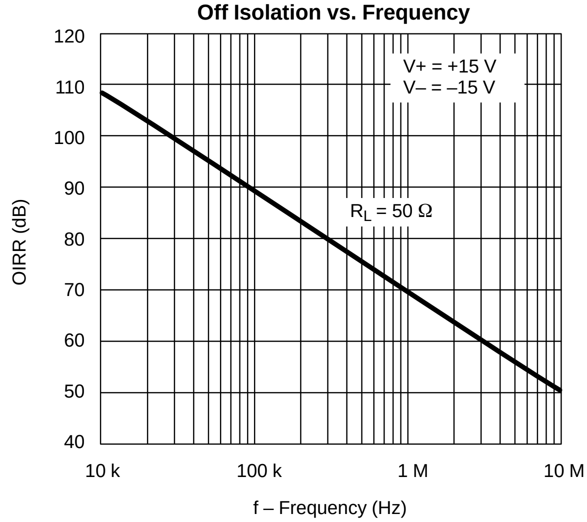
Leakage Current vs. Temperature



Q_S, Q_D – Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency



TEST CIRCUITS

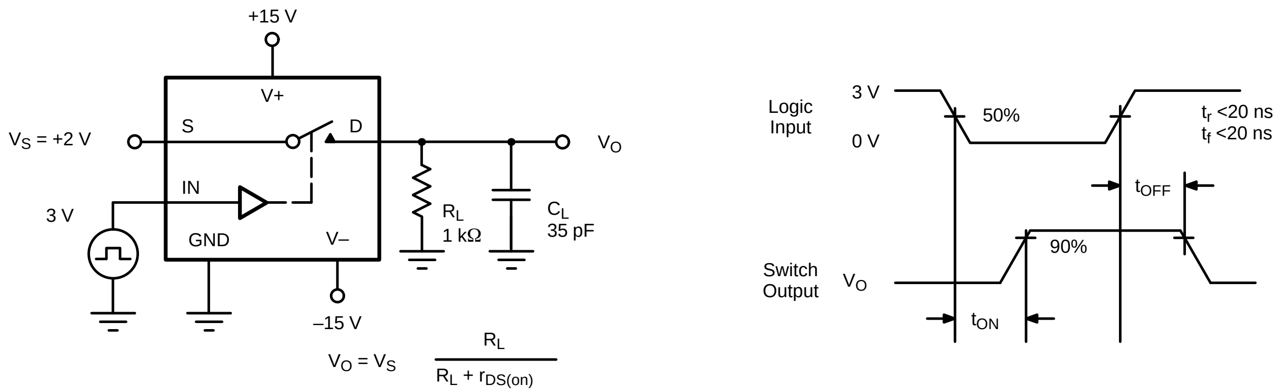


FIGURE 2. Switching Time

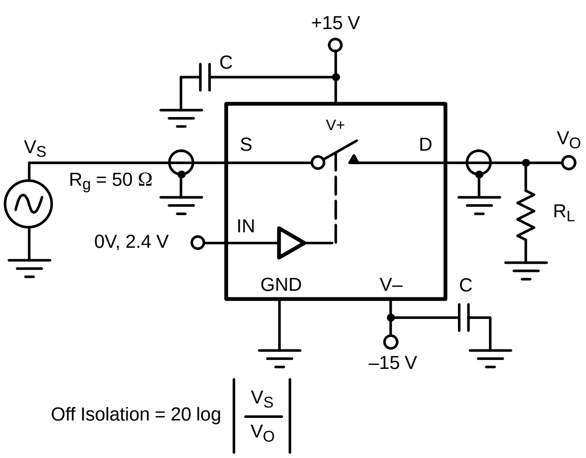


FIGURE 3. Off Isolation

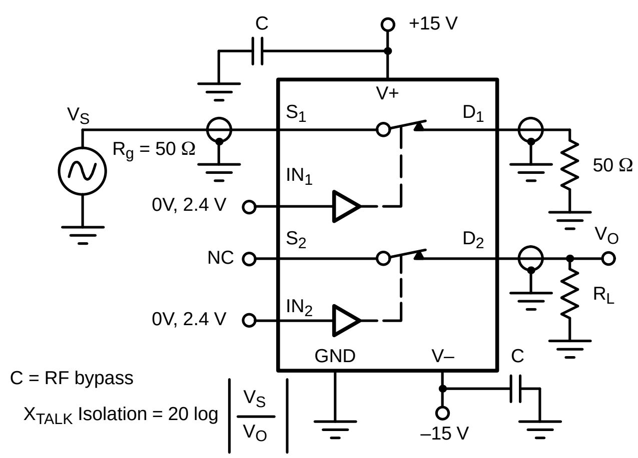


FIGURE 4. Channel-to-Channel Crosstalk

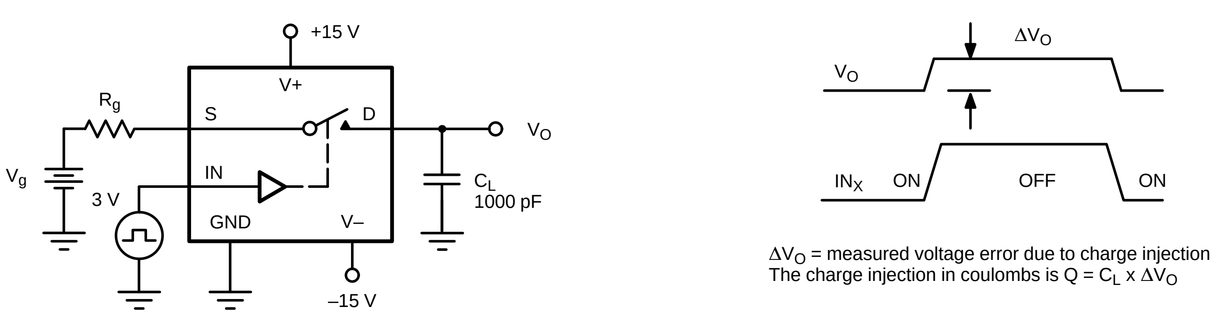


FIGURE 5. Charge Injection

APPLICATIONS

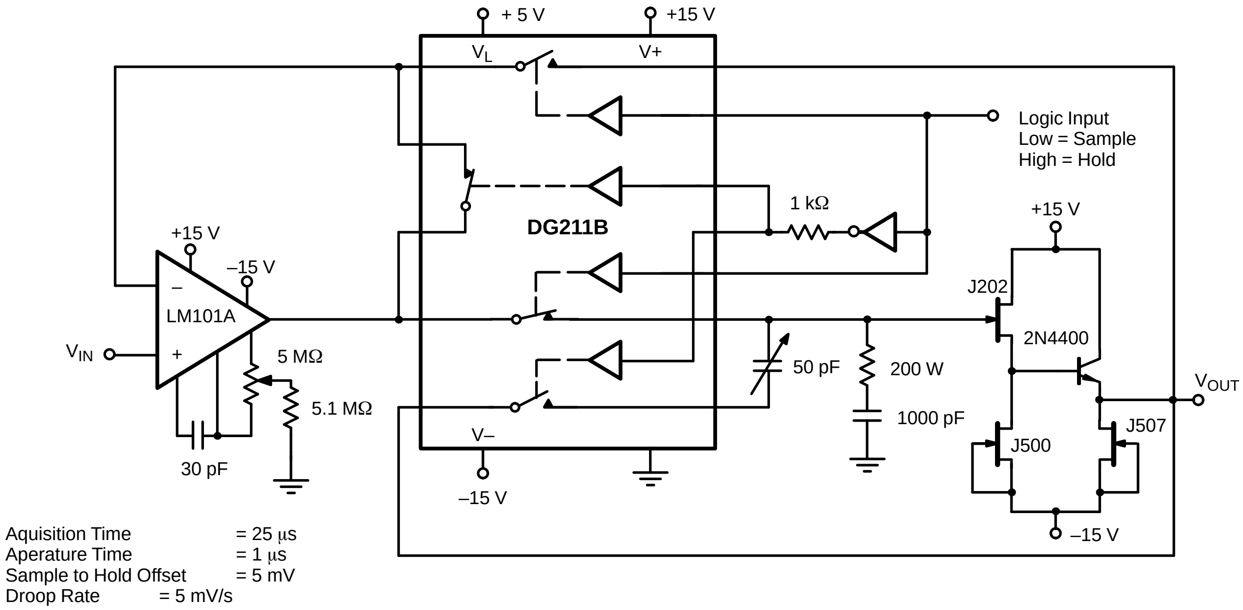
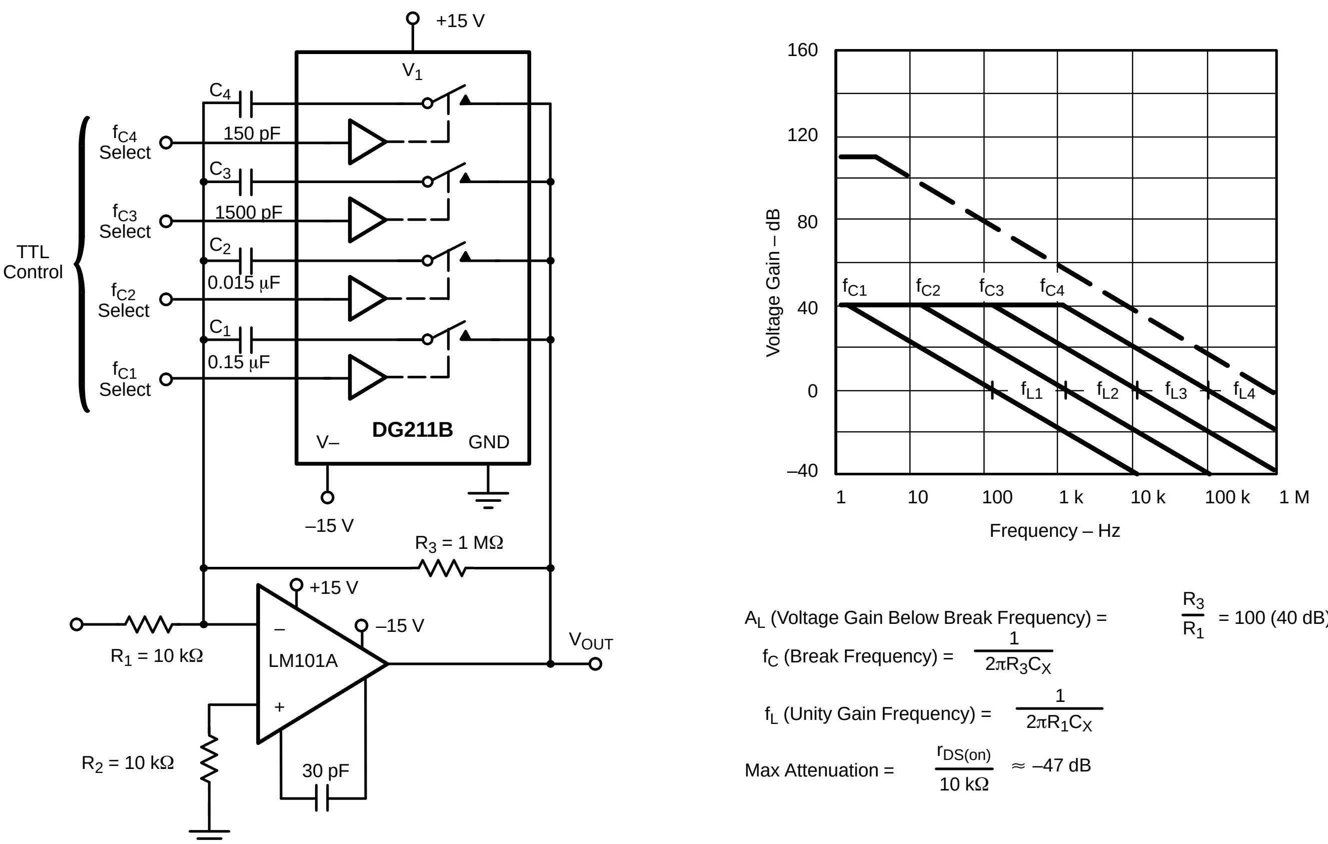


FIGURE 6. Sample-and-Hold



A_L (Voltage Gain Below Break Frequency) = $\frac{R_3}{R_1}$ = 100 (40 dB)

f_C (Break Frequency) = $\frac{1}{2\pi R_3 C_X}$

f_L (Unity Gain Frequency) = $\frac{1}{2\pi R_1 C_X}$

Max Attenuation = $\frac{r_{DS(on)}}{10\ k\Omega} \approx -47$ dB

FIGURE 7. Active Low Pass Filter with Digitally Selected Break Frequency

APPLICATIONS

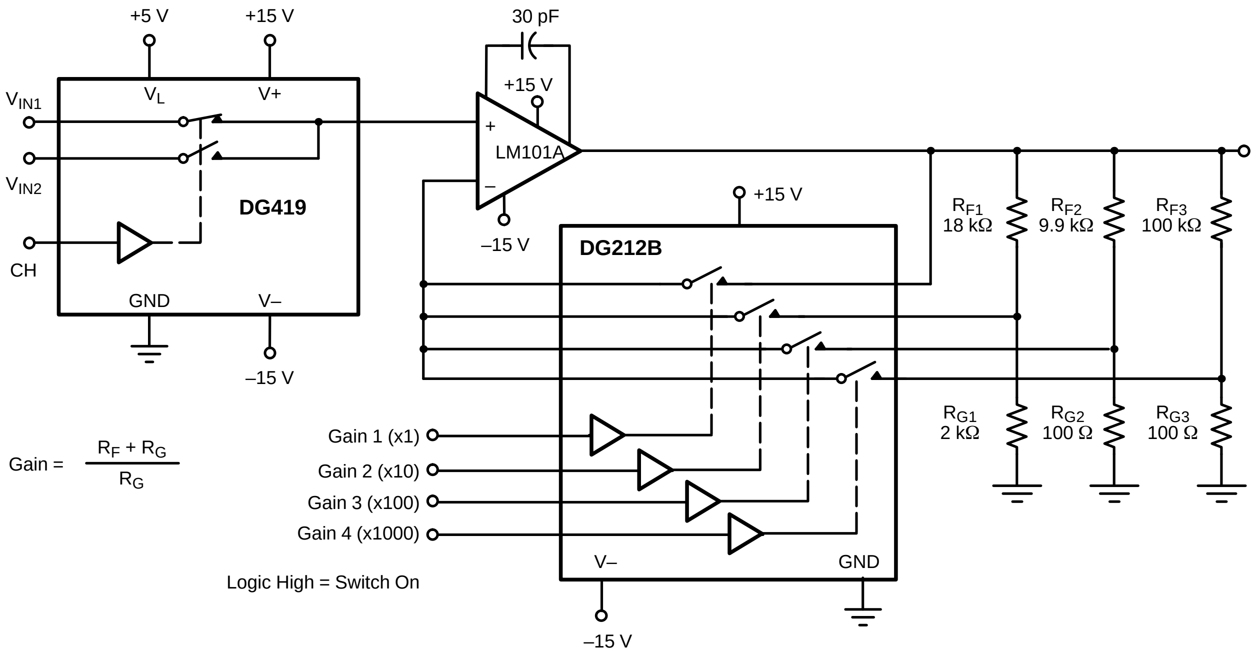


FIGURE 8. A Precision Amplifier with Digitally Programable Input and Gains

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