

## **FDS8958A**

# Dual N & P-Channel PowerTrench<sup>O</sup> MOSFET

### **General Description**

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state ressitance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### **Features**

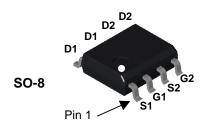
Q1: N-Channel

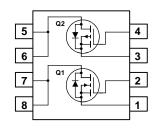
7.0A, 30V 
$$R_{DS(on)} = 0.028\Omega$$
 @  $V_{GS} = 10V$   $R_{DS(on)} = 0.040\Omega$  @  $V_{GS} = 4.5V$ 

Q2: P-Channel

-5A, -30V 
$$R_{DS(on)} = 0.052\Omega @ V_{GS} = -10V$$
 
$$R_{DS(on)} = 0.080\Omega @ V_{GS} = -4.5V$$

- Fast switching speed
- High power and handling capability in a widely used surface mount package





### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	7	-5	Α
	- Pulsed		20	-20	
P <sub>D</sub>	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation (Note 1a)		1.6		
		(Note 1b)		1	
		(Note 1c)	C	.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150		°C

### **Thermal Characteristics**

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8958A	FDS8958A	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Off Cha	racteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_D = 250 \mu\text{A} \ V_{GS} = 0 \text{ V}, \qquad I_D = -250 \mu\text{A}$	Q1 Q2	30 -30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C $I_D$ = -250 μA, Referenced to 25°C	Q1 Q2		25 -23		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \qquad V_{GS} = 0 \text{ V} $ $V_{DS} = -24 \text{ V}, \qquad V_{GS} = 0 \text{ V}$	Q1 Q2			1 -1	μА
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$	All			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$	All			-100	nA
On Cha	racteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS},$ $I_{D} = 250 \ \mu A$ $V_{DS} = V_{GS},$ $I_{D} = -250 \ \mu A$	Q1 Q2	1 -1	1.9 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C $I_D$ = -250 $\mu$ A, Referenced to 25°C	Q1 Q2		-4.5 4.5		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$\begin{array}{llllllllllllllllllllllllllllllllllll$	Q1		19 27 24	28 42 40	mΩ
		$ \begin{array}{llllllllllllllllllllllllllllllllllll$	Q2		42 57 65	52 78 80	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10 \text{ V}, \qquad V_{DS} = 5 \text{ V} $ $V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	Q1 Q2	20 -20			Α
<b>G</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V},$ $I_{D} = 7 \text{ A}$ $V_{DS} = -5 \text{ V},$ $I_{D} = -5 \text{ A}$	Q1 Q2		25 10		S
Dynami	c Characteristics						
C <sub>iss</sub>	Input Capacitance	Q1 $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	Q1 Q2		575 528		pF
Coss	Output Capacitance	Q2	Q1 Q2		145 132		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	Q1 Q2		65 70		pF
R <sub>G</sub>	Gate Resistance	$V_{GS} = 15 \text{ mV}, \qquad f = 1.0 \text{ MHz}$	Q1 Q2		2.1 6.0		Ω

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Switchir	ng Characteristics (Note	2)					
t <sub>d(on)</sub>	Turn-On Delay Time	Q1	Q1		8	16	ns
- (- )	•	$V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$	Q2		7	14	
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10V$ , $R_{GEN} = 6 \Omega$	Q1		5	10	ns
			Q2		13	24	
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2	Q1		23	37	ns
,	•	$V_{DD} = -15 \text{ V}, I_{D} = -1 \text{ A},$	Q2		14	25	
t <sub>f</sub>	Turn-Off Fall Time	$V_{GS} = -10V$ , $R_{GEN} = 6 \Omega$	Q1		3	6	ns
			Q2		9	17	
Qg	Total Gate Charge	Q1	Q1		10.7	26	nC
-	_	$V_{DS} = 15 \text{ V}, I_{D} = 7 \text{ A}, V_{GS} = 10 \text{ V}$	Q2		9.6	13	
$Q_{gs}$	Gate-Source Charge		Q1		1.7		nC
_	_	Q2	Q2		2.2		
$Q_{gd}$	Gate-Drain Charge	$V_{DS} = -15 \text{ V}, I_{D} = -5 \text{ A}, V_{GS} = -10 \text{ V}$	Q1		2.1		nC
-	_		Q2		1.7		
Drain-S	Source Diode Character	istics and Maximum Rating	S				
Is	Maximum Continuous Drain-S	Source Diode Forward Current	Q1			1.3	Α
o .			Q2			-1.3	
V <sub>SD</sub>	Drain-Source Diode Forward	$V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A}$ (Note 2)	Q1		0.75	1.2	V
	Voltage	$V_{GS} = 0 \text{ V}, I_S = -1.3 \text{ A}$ (Note 2)	Q2		-0.88	-1.2	
t <sub>rr</sub>	Diode Reverse Recovery	Q1	Q1		19		nS
	Time	$I_F = 7 \text{ A}, d_{iF}/d_t = 100 \text{ A/µs}$	Q2		19		
Q <sub>rr</sub>	Diode Reverse Recovery	Q2	Q1		9		nC
**	Charge	$I_F = -5 \text{ A}, d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$	Q2		6		

#### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°/W when mounted on a .02 in² pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## **Typical Characteristics: Q1 (N-Channel)**

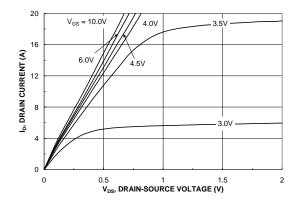


Figure 1. On-Region Characteristics.

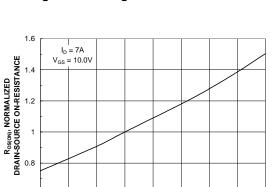


Figure 3. On-Resistance Variation with Temperature.

-50

-25

0 25 50 75 100 T<sub>J</sub>, JUNCTION TEMPERATURE (°C) 125

150

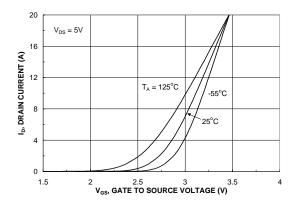


Figure 5. Transfer Characteristics.

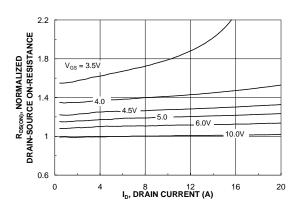


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

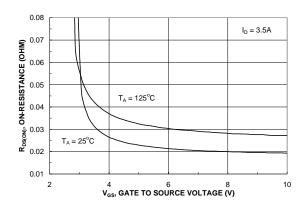


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

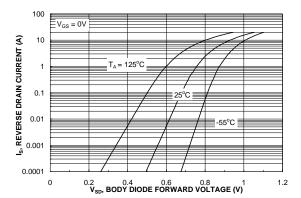


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics: Q1 (N-Channel)

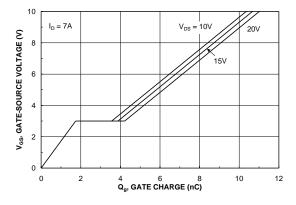


Figure 7. Gate Charge Characteristics.

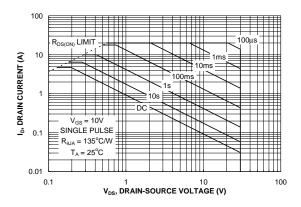


Figure 9. Maximum Safe Operating Area.

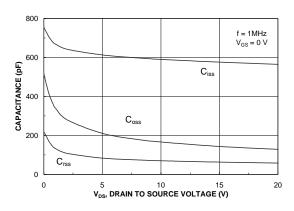


Figure 8. Capacitance Characteristics.

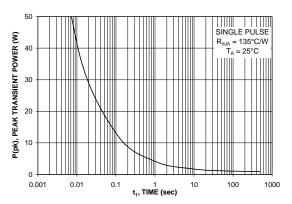


Figure 10. Single Pulse Maximum Power Dissipation.

## Typical Characteristics: Q2 (P-Channel)

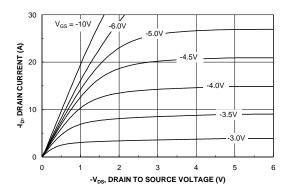


Figure 11. On-Region Characteristics.

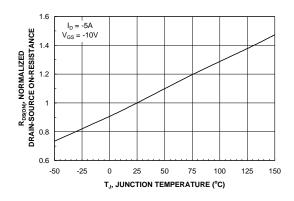


Figure 13. On-Resistance Variation with Temperature.

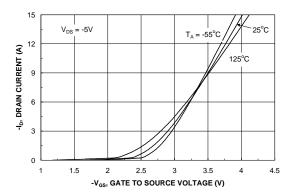


Figure 15. Transfer Characteristics.

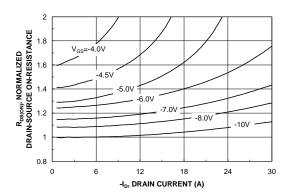


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

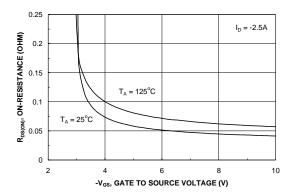


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

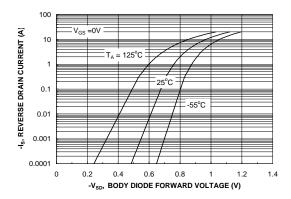
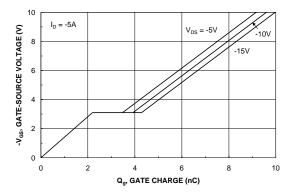


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics: Q2 (P-Channel)



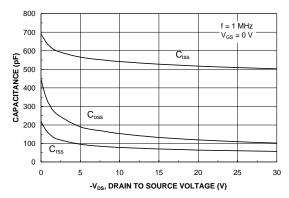
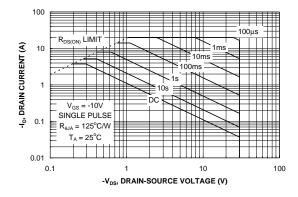


Figure 17. Gate Charge Characteristics.





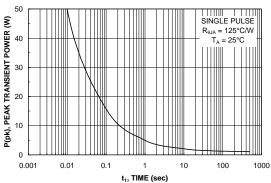


Figure 18. Capacitance Characteristics.

Figure 19. Maximum Safe Operating Area.



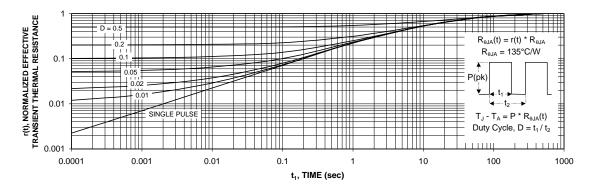


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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