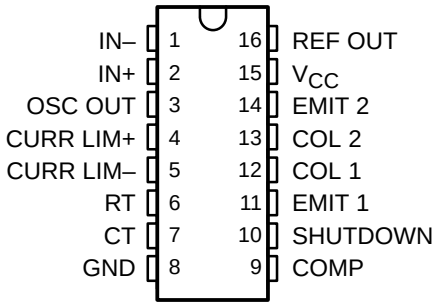
SLVS077D – APRIL 1977 – REVISED FEBRUARY 2003

- **Complete Pulse-Width Modulation (PWM) Power-Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Industry Standard SG2524 and SG3524**

SG2524 . . . D OR N PACKAGE
SG3524 . . . D, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

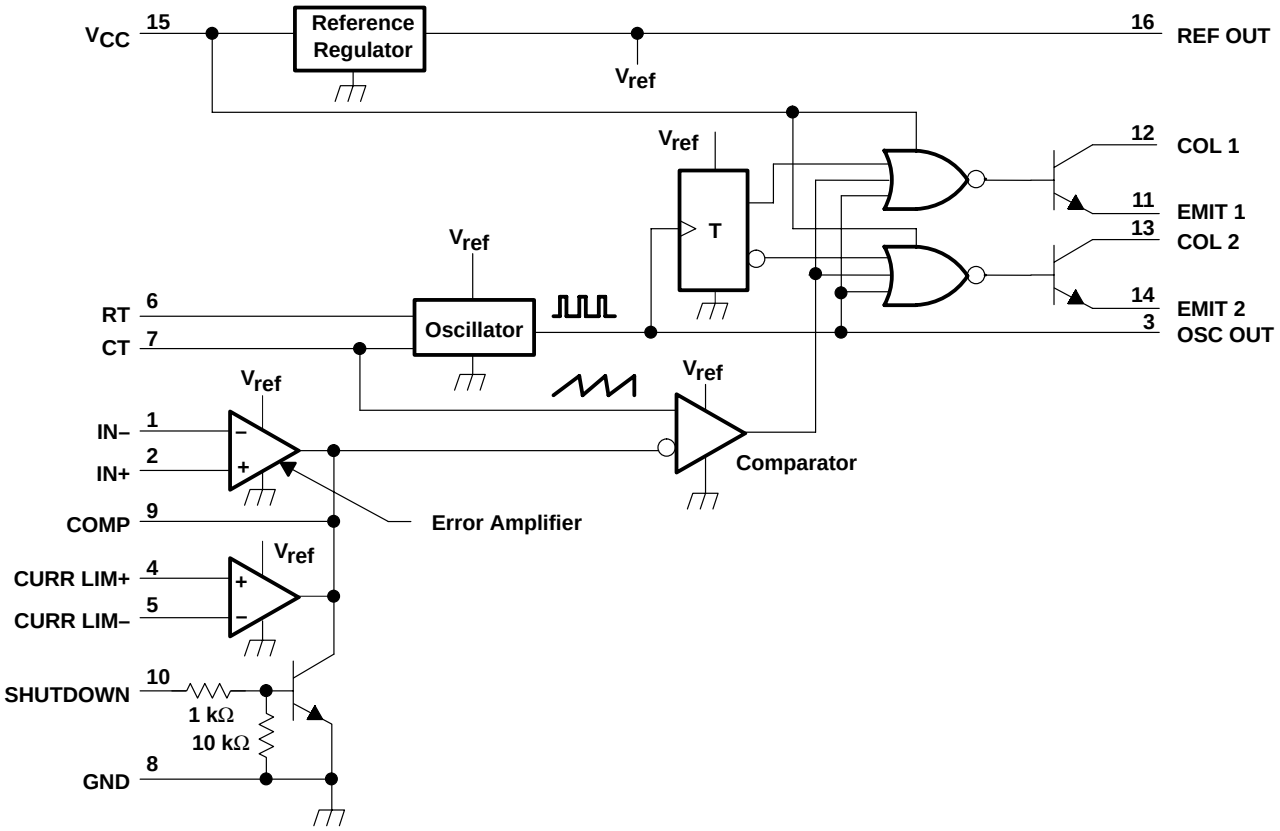
The SG2524 and SG3524 incorporate all the functions required in the construction of a regulating power supply, inverter, or switching regulator on a single chip. They also can be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity-converter applications employing fixed-frequency, pulse-width modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shutdown circuitry.

ORDERING INFORMATION

T_A	INPUT REGULATION MAX (mV)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	30	PDIP (N)	Tube of 25	SG3524N	SG3524N
		SOIC (D)	Tube of 40	SG3524D	SG3524
			Reel of 2500	SG3524DR	
		SOP (NS)	Reel of 2000	SG3524NSR	SG3524
–25°C to 85°C	20	PDIP (N)	Tube of 25	SG2524N	SG2524N
		SOIC (D)	Tube of 40	SG2524D	SG2524
			Reel of 2500	SG2524DR	

† Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



NOTE A: Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Notes 1 and 2)	40 V
Collector output current, I_{CC}	100 mA
Reference output current, $I_{O(ref)}$	50 mA
Current through CT terminal	–5 mA
Operating virtual junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the V_{CC} and reference output (REF OUT) pin both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.
3. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operation at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		8	40	V
	Reference output current		0	50	mA
	Current through CT terminal		–0.03	–2	mA
R_T	Timing resistor		1.8	100	kΩ
C_T	Timing capacitor		0.001	0.1	μF
T_A	Operating free-air temperature	SG2524	–25	85	°C
		SG3524	0	70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.6	5	5.4	V
Input regulation	V_{CC} = 8 V to 40 V		10	20		10	30	mV
Ripple rejection	f = 120 Hz		66			66		dB
Output regulation	I_O = 0 mA to 20 mA		20	50		20	50	mV
Output voltage change with temperature	T_A = MIN to MAX		0.3%	1%		0.3%	1%	
Short-circuit output current§	V_{ref} = 0		100			100		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

oscillator section

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
f_{osc}	Oscillator frequency	C_T = 0.001 μF,	R_T = 2 kΩ		450		kHz
	Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant			5%		
Δf_{osc}	Frequency change with voltage	V_{CC} = 8 V to 40 V,	T_A = 25°C			1%	
	Frequency change with temperature	T_A = MIN to MAX				2%	
	Output amplitude at OSC OUT	T_A = 25°C			3.5		V
t_w	Output pulse duration (width) at OSC OUT	C_T = 0.01 μF,	T_A = 25°C		0.5		μs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

error amplifier section

PARAMETER		TEST CONDITIONS†	SG2524			SG3524			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10	mV
I_{IB}	Input bias current	V_{IC} = 2.5 V		2	10		2	10	μA
	Open-loop voltage amplification		72	80		60	80		dB
V_{ICR}	Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4			V
CMMR	Common-mode rejection ratio			70			70		dB
B_1	Unity-gain bandwidth			3			3		MHz
	Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	V

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C

output section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{(BR)CE}$	Collector-emitter breakdown voltage		40			V
	Collector off-state current	V_{CE} = 40 V		0.01	50	μA
V_{sat}	Collector-emitter saturation voltage	I_C = 50 mA		1	2	V
V_O	Emitter output voltage	V_C = 20 V, I_E = –250 μA	17	18		V
t_r	Turn-off voltage rise time	R_C = 2 kΩ		0.2		μs
t_f	Turn-on voltage fall time	R_C = 2 kΩ		0.1		μs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

comparator section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
	Maximum duty cycle, each output		45%			
V_{IT}	Input threshold voltage at COMP	Zero duty cycle		1		V
		Maximum duty cycle		3.5		
I_{IB}	Input bias current			–1		μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

current limiting section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_I	Input voltage range (either input)		–1 to1			V
$V_{(SENSE)}$	Sense voltage at T_A = 25°C	$V_{(IN+)} - V_{(IN-)} \geq 50$ mV, $V_{(COMP)}$ = 2 V	175	200	225	mV
	Temperature coefficient of sense voltage			0.2		mV/°C

‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{st}	Standby current	V_{CC} = 40 V, IN–, CURR LIM+, C_T, GND, COMP, EMIT 1, EMIT 2 grounded, IN+ at 2 V, All other inputs and outputs open		8	10	mA

‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

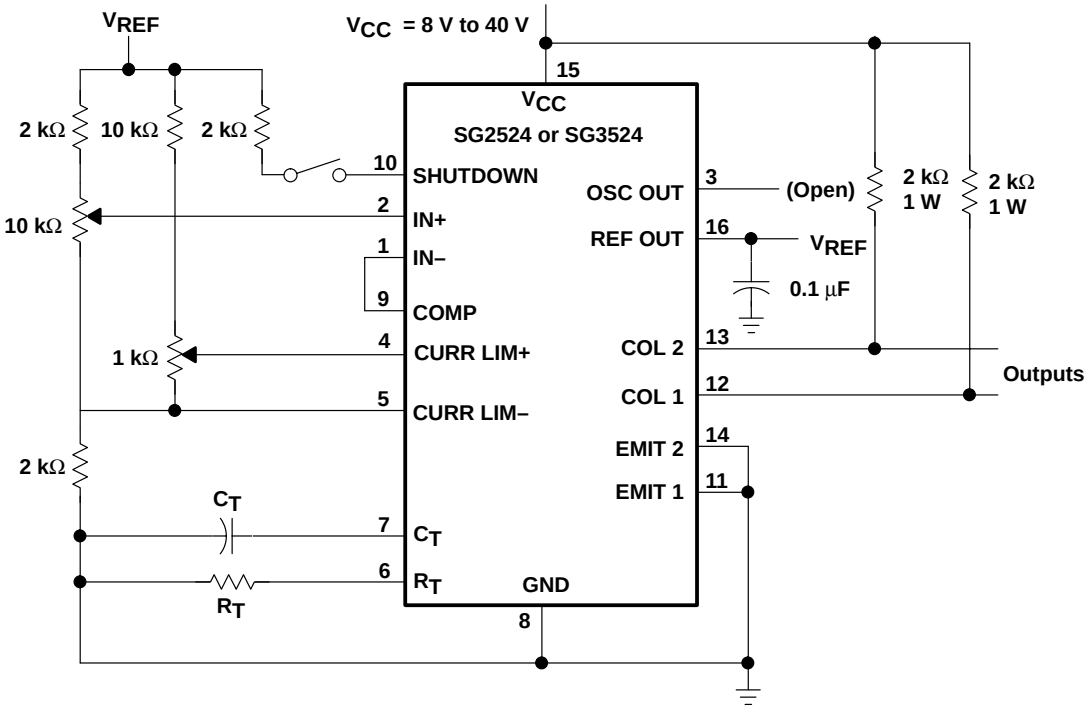


Figure 1. General Test Circuit

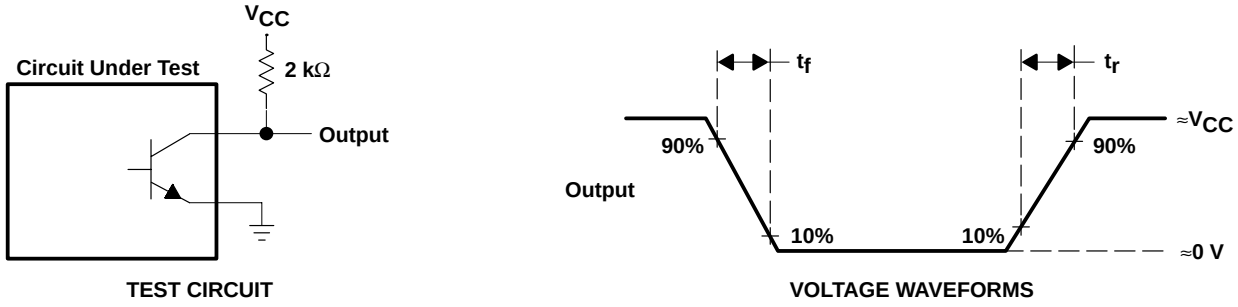


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION OF ERROR AMPLIFIER vs FREQUENCY

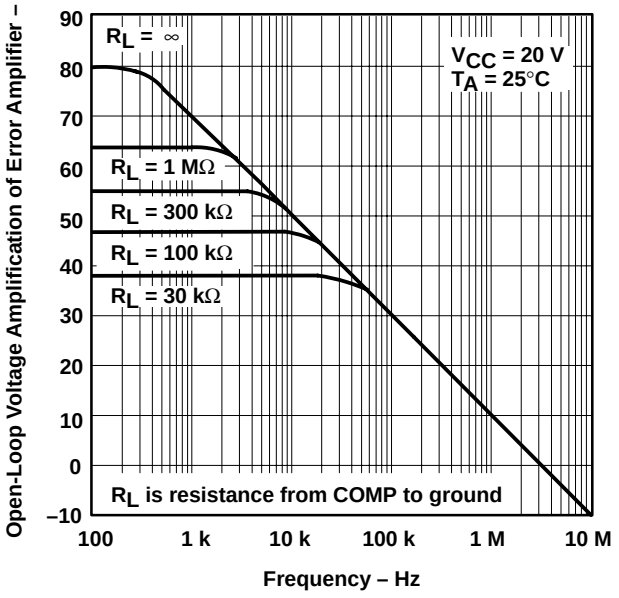


Figure 3

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

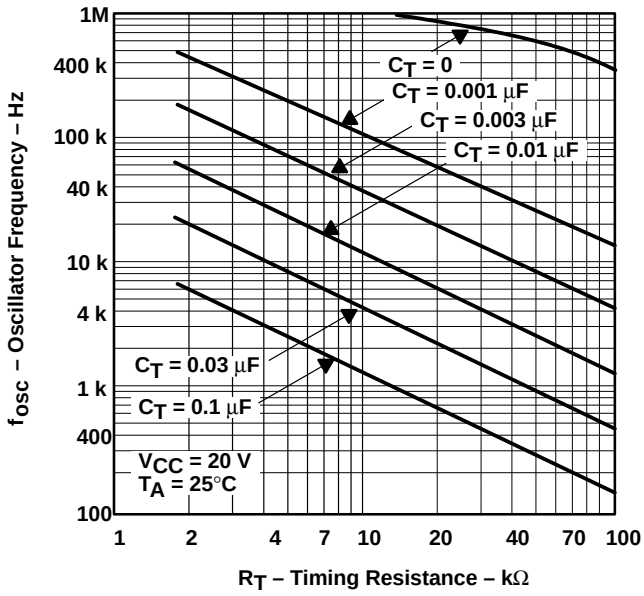


Figure 4

OUTPUT DEAD TIME vs TIMING CAPACITANCE

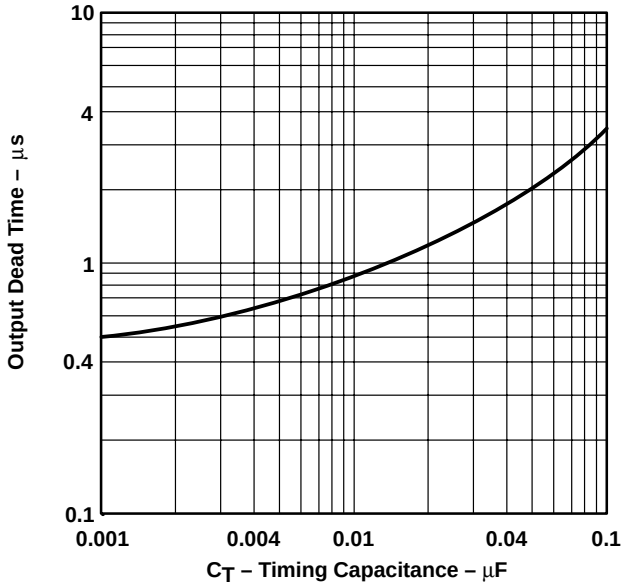


Figure 5

PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation (PWM) voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor, R_T, and one timing capacitor, C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator, providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an onboard 5-V regulator that serves as a reference, as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference can be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator then is steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is one-half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is pinned out externally via the COMP pin, which can be employed to either control the gain of the error amplifier or to compensate it. In addition, the COMP pin can be used to provide additional control to the regulator.

APPLICATION INFORMATION†

oscillator

The oscillator controls the frequency of the SG2524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.30}{R_T C_T}$$

where: R_T is in kΩ
C_T is in μF
f is in kHz

Practical values of C_T fall between 0.001 μF and 0.1 μF. Practical values of R_T fall between 1.8 kΩ and 100 kΩ. This results in a frequency range typically from 130 Hz to 722 kHz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse duration can be maintained by applying a shunt capacitance from OSC OUT to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, R_TC_T must be selected for a clock period slightly greater than that of the external clock.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

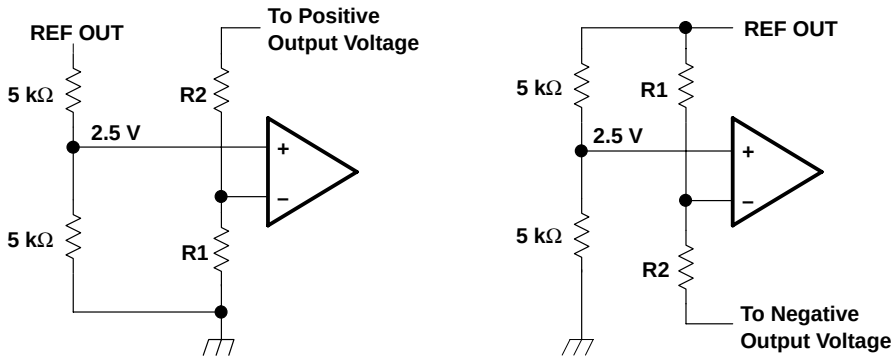
APPLICATION INFORMATION†

synchronous operation (continued)

If two or more SG2524 regulators are operated synchronously, all oscillator output terminals must be tied together. The oscillator programmed for the minimum clock period is the master from which all the other SG2524s operate. In this application, the C_TR_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and, subsequently, resets the slave regulators.

voltage reference

The 5-V internal reference can be employed by use of an external resistor divider network to establish a reference common-mode voltage range (1.8 V to 3.4 V) within the error amplifiers (see Figure 6), or an external reference can be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference can be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.



$$V_O = 2.5\ V \frac{R1 + R2}{R1} \qquad V_O = 2.5\ V \left(1 - \frac{R2}{R1}\right)$$

Figure 6. Error-Amplifier Bias Circuits

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node (R_L = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and easily can be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

compensation

COMP, as previously discussed, is made available for compensation. Since most output filters introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can be accomplished best with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 μF. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

shutdown circuitry

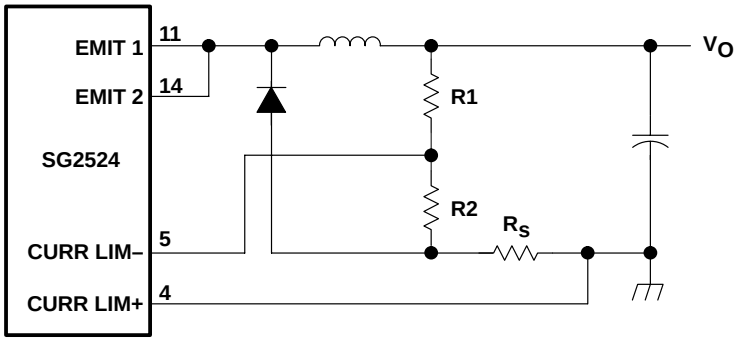
COMP also can be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and, thus, disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM– also can be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM– also can be grounded to convert CURR LIM+ into an additional shutdown terminal.

current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV ±25 mV and must be applied in the ground line since the voltage range of the inputs is limited to 1 V to –1 V. Caution should be taken to ensure the –1-V limit is not exceeded by either input, otherwise, damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.



$$I_{O(max)} = \frac{1}{R_S}\left(200\ mV + \frac{V_O\ R2}{R1 + R2}\right)$$

$$I_{OS} = \frac{200\ mV}{R_S}$$

Figure 7. Foldback Current Limiting for Shorted Output Conditions

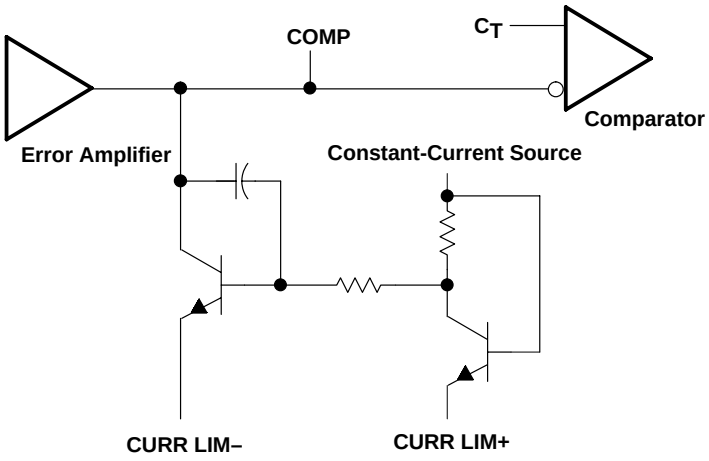


Figure 8. Current-Limit Schematic

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

output circuitry

The SG2524 contains two identical npn transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage-regulator control circuit. They can be segregated into three basic categories:

- Capacitor-diode-coupled voltage multipliers
- Inductor-capacitor-implemented single-ended circuits
- Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10, and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12–15.

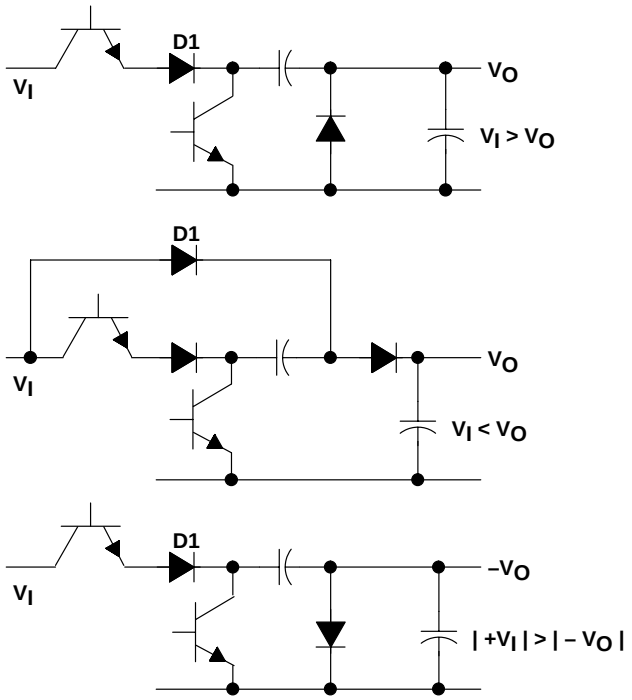


Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

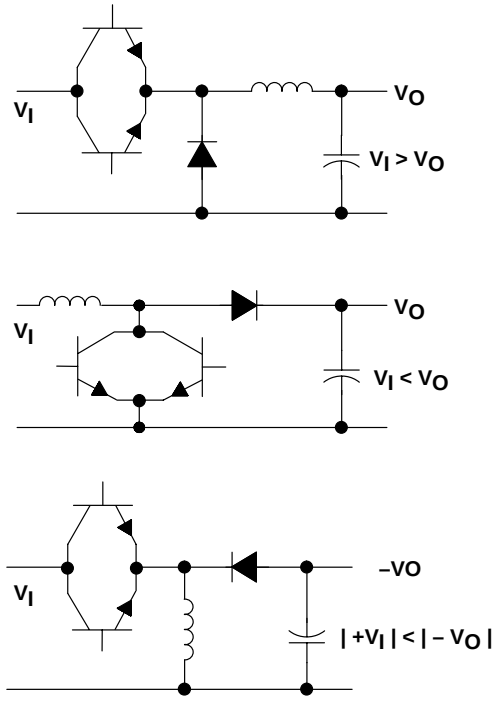
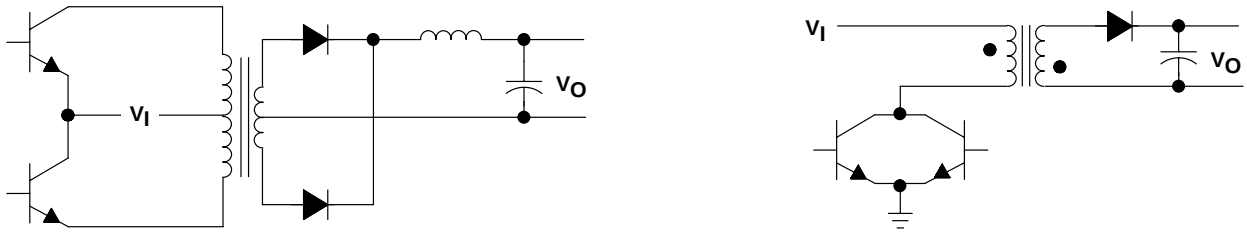


Figure 10. Single-Ended Inductor Circuit



Push-Pull **Flyback**

Figure 11. Transformer-Coupled Outputs

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

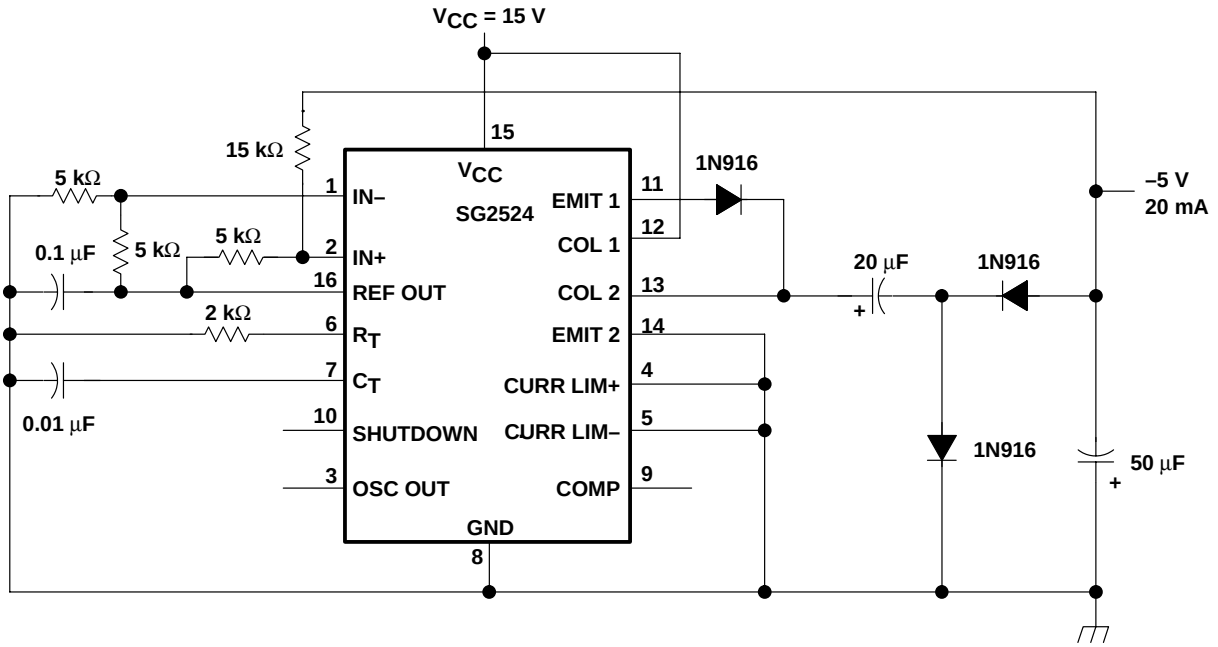


Figure 12. Capacitor-Diode Output Circuit

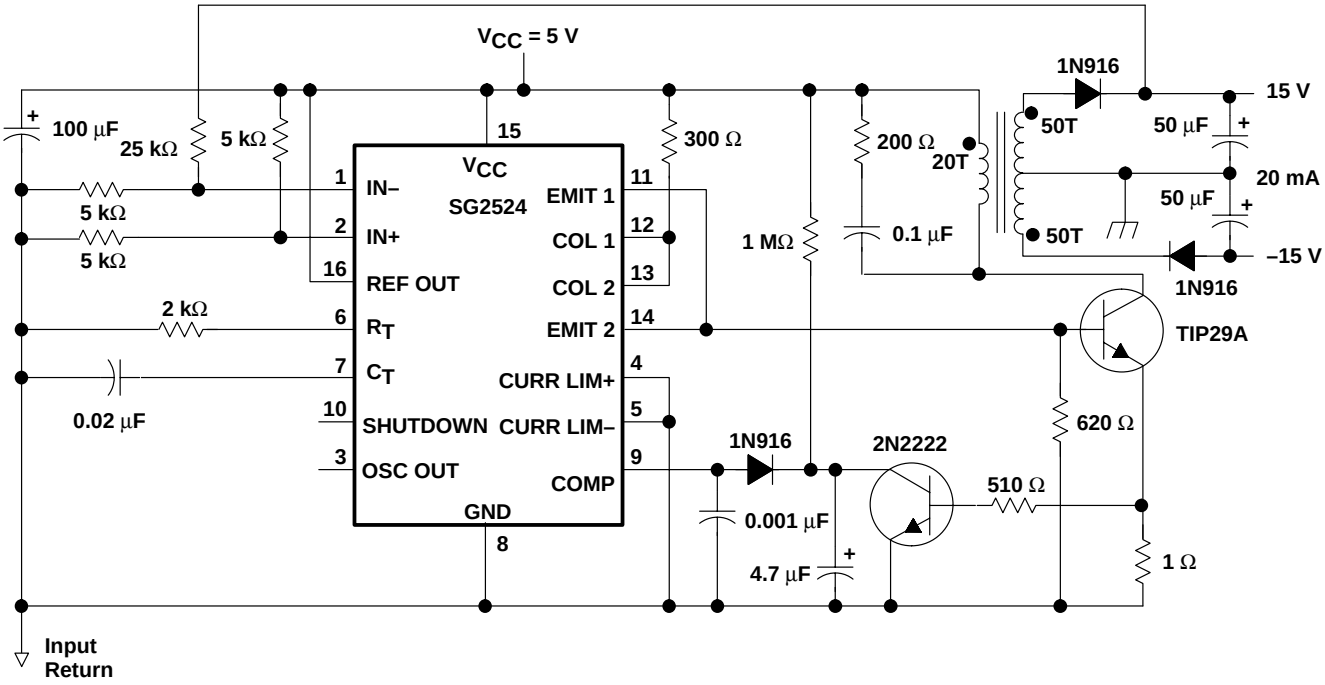


Figure 13. Flyback Converter Circuit

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

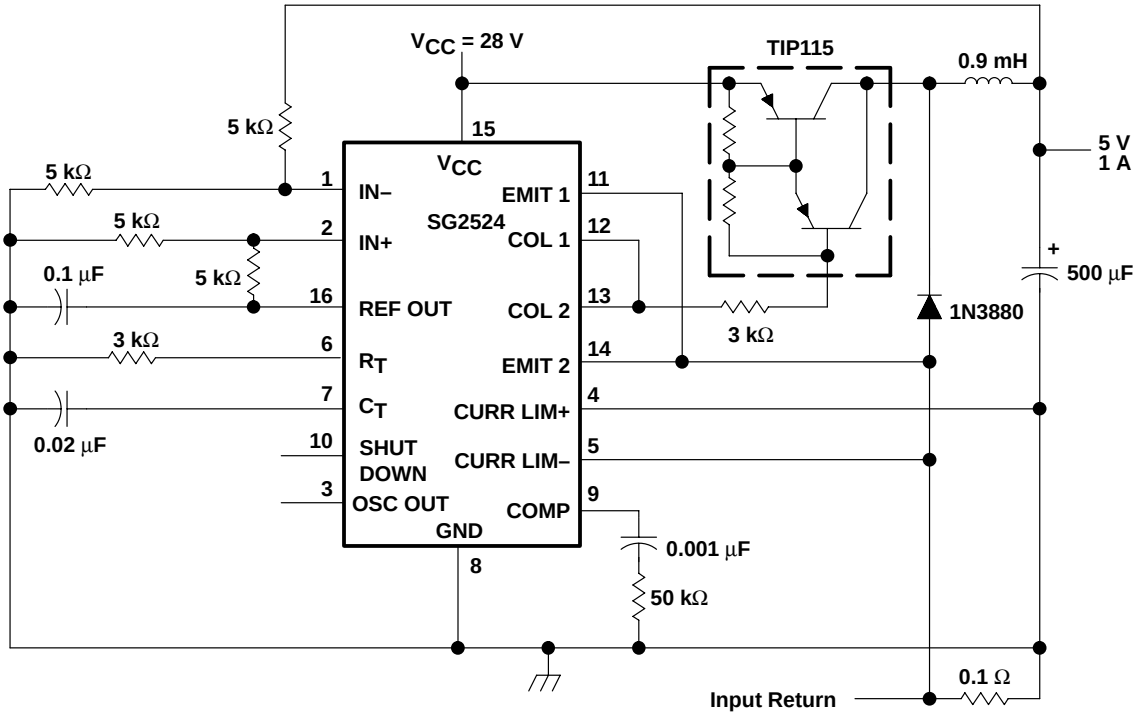


Figure 14. Single-Ended LC Circuit

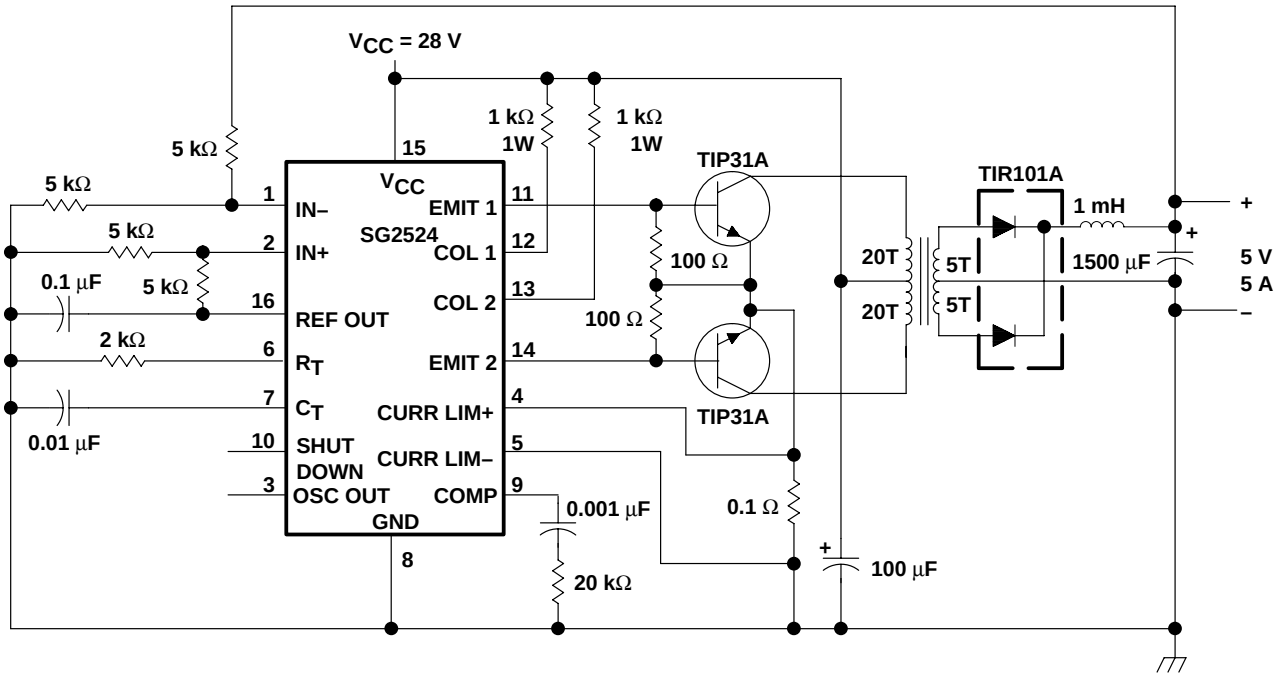


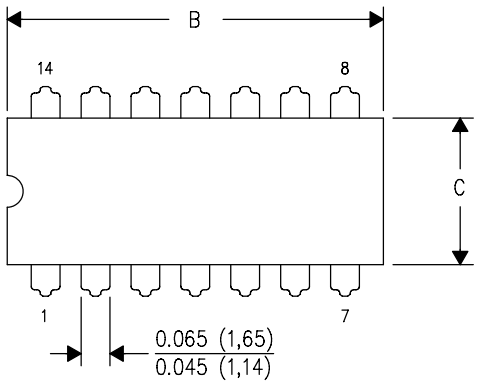
Figure 15. Push-Pull Transformer-Coupled Circuit

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

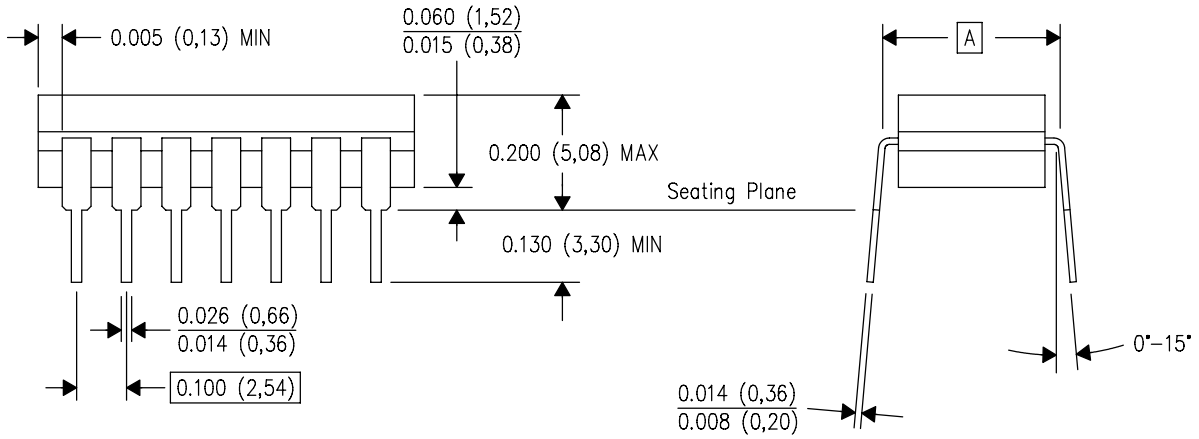
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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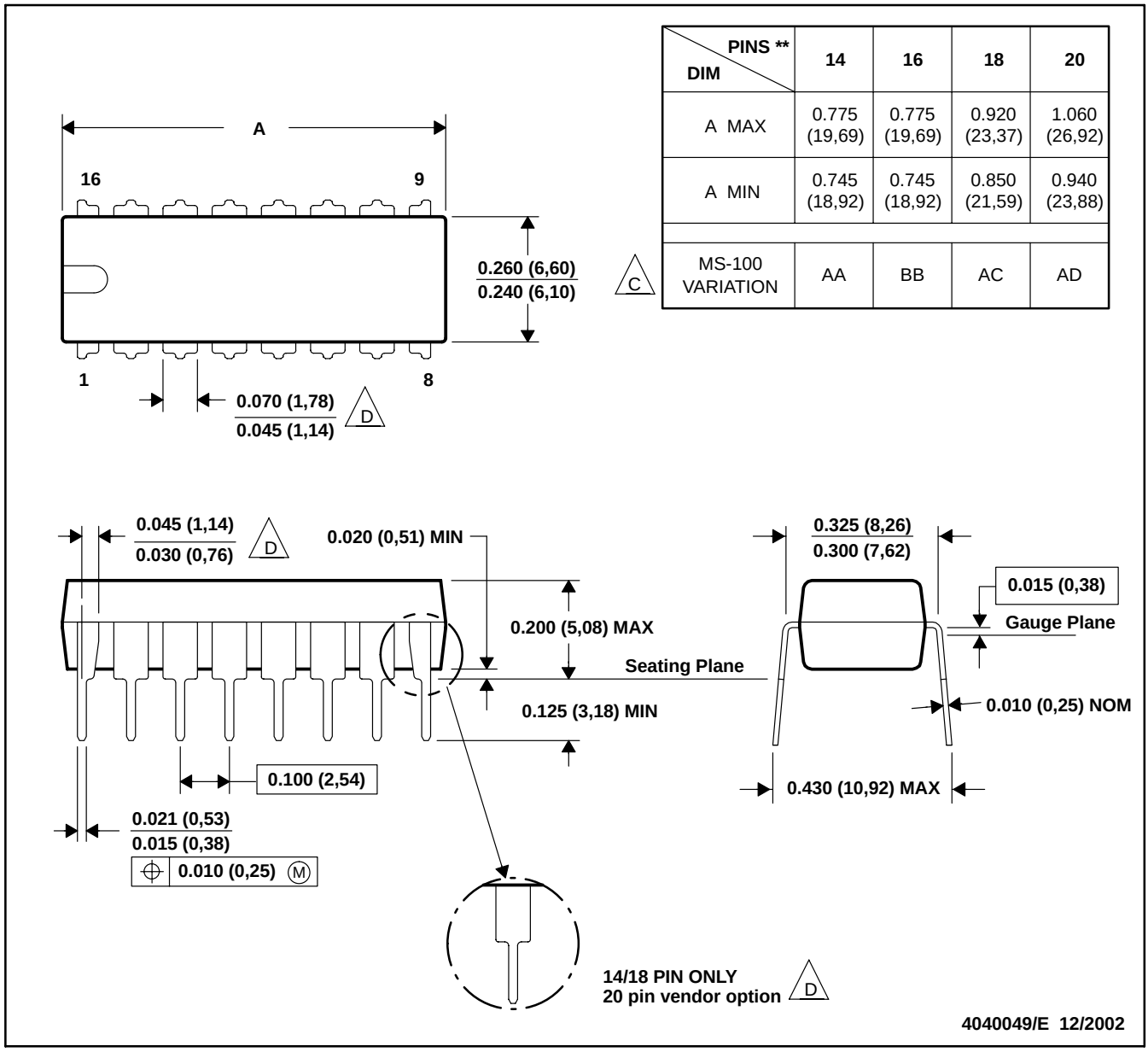
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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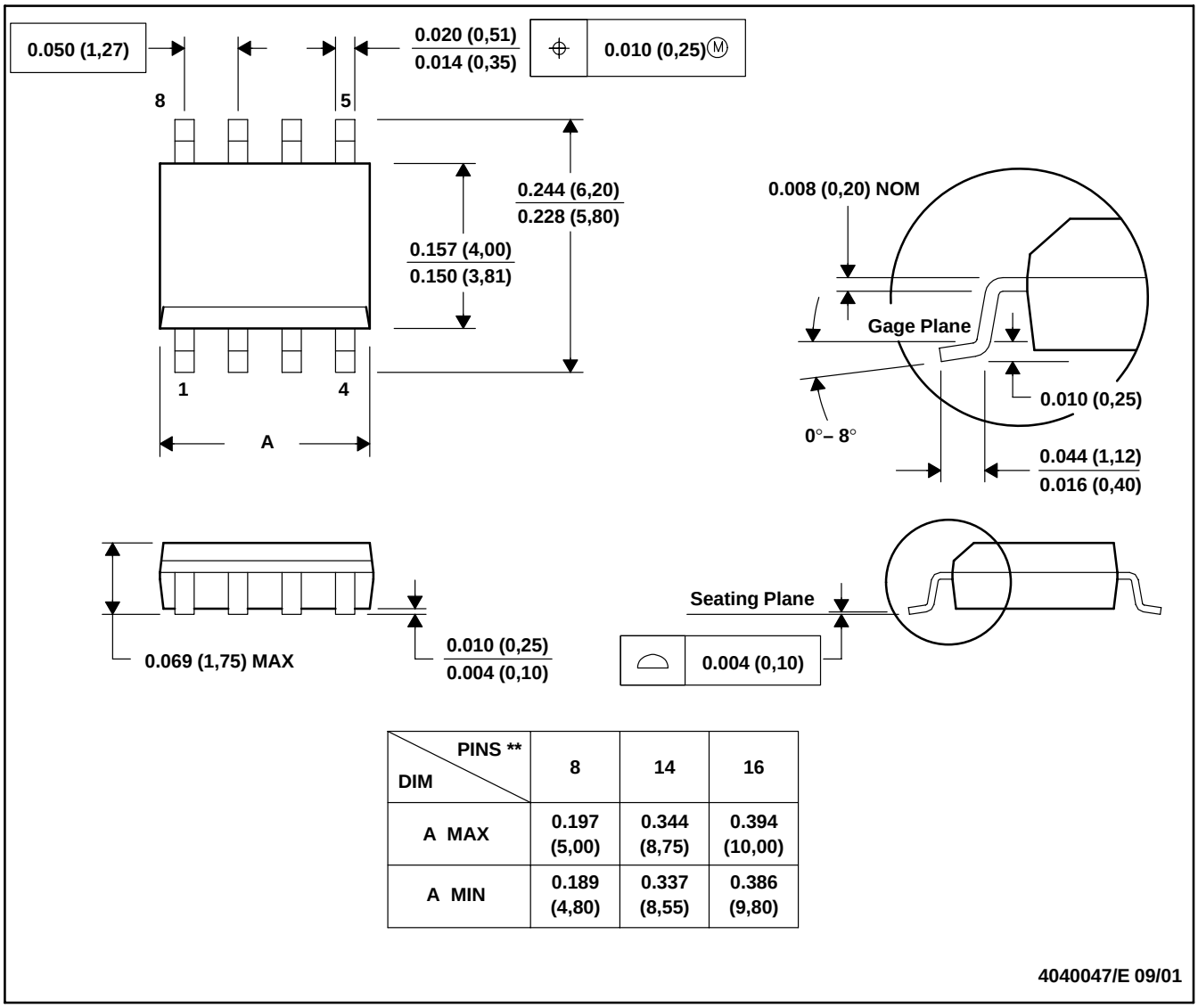
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

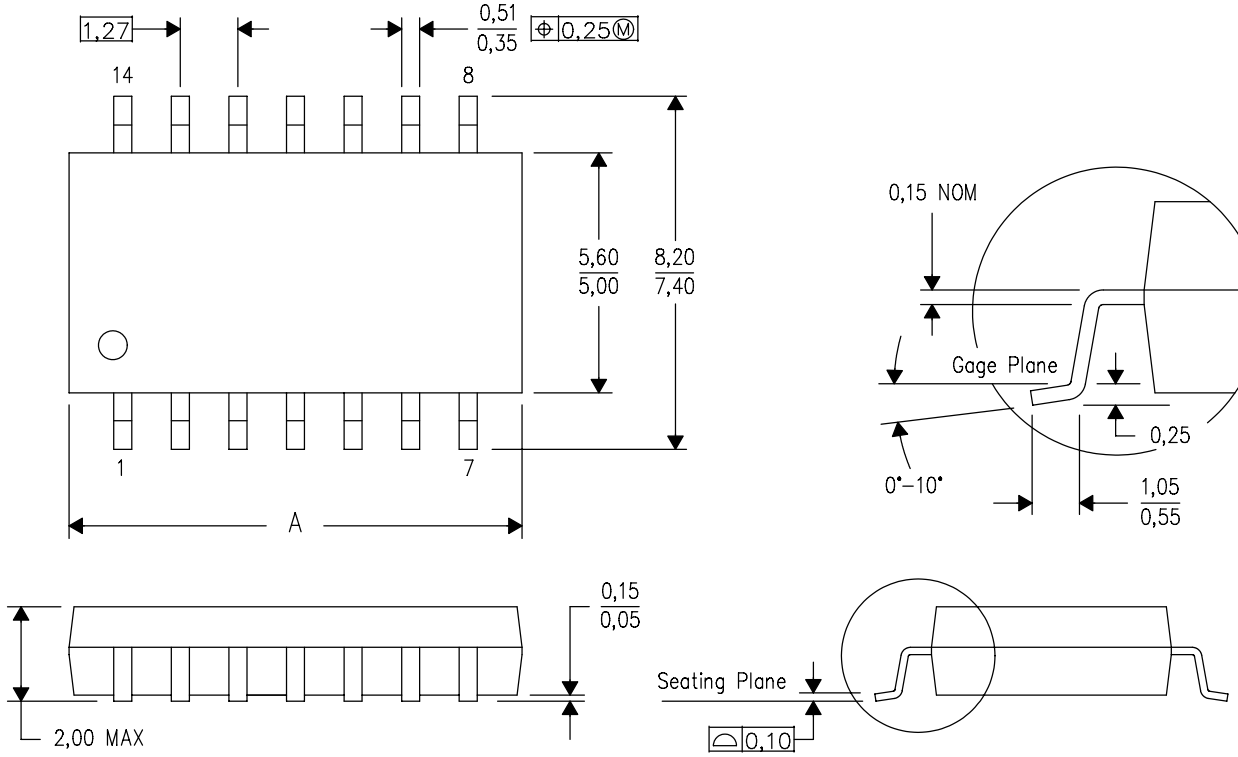
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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